

# SERVICE MANUAL

*notebook*

P957HP6

[www.aitech1.ru](http://www.aitech1.ru)



# Appendix B: Schematic Diagrams

This appendix has circuit diagrams of the **P957HP6** notebook's PCB's. The following table indicates where to find the appropriate schematic diagram.

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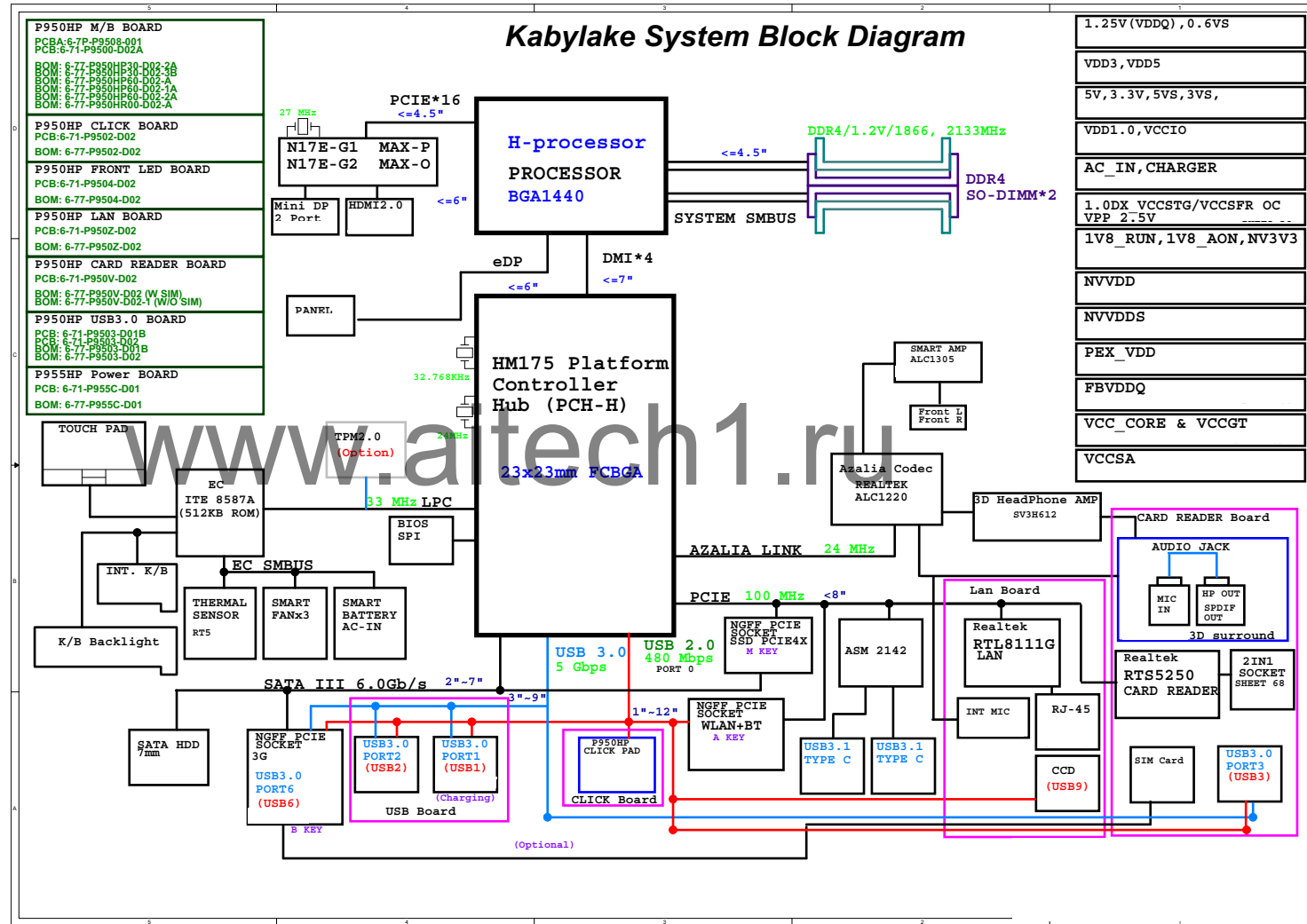
Table B - 1  
**SCHEMATIC  
DIAGRAMS**



## Version Note

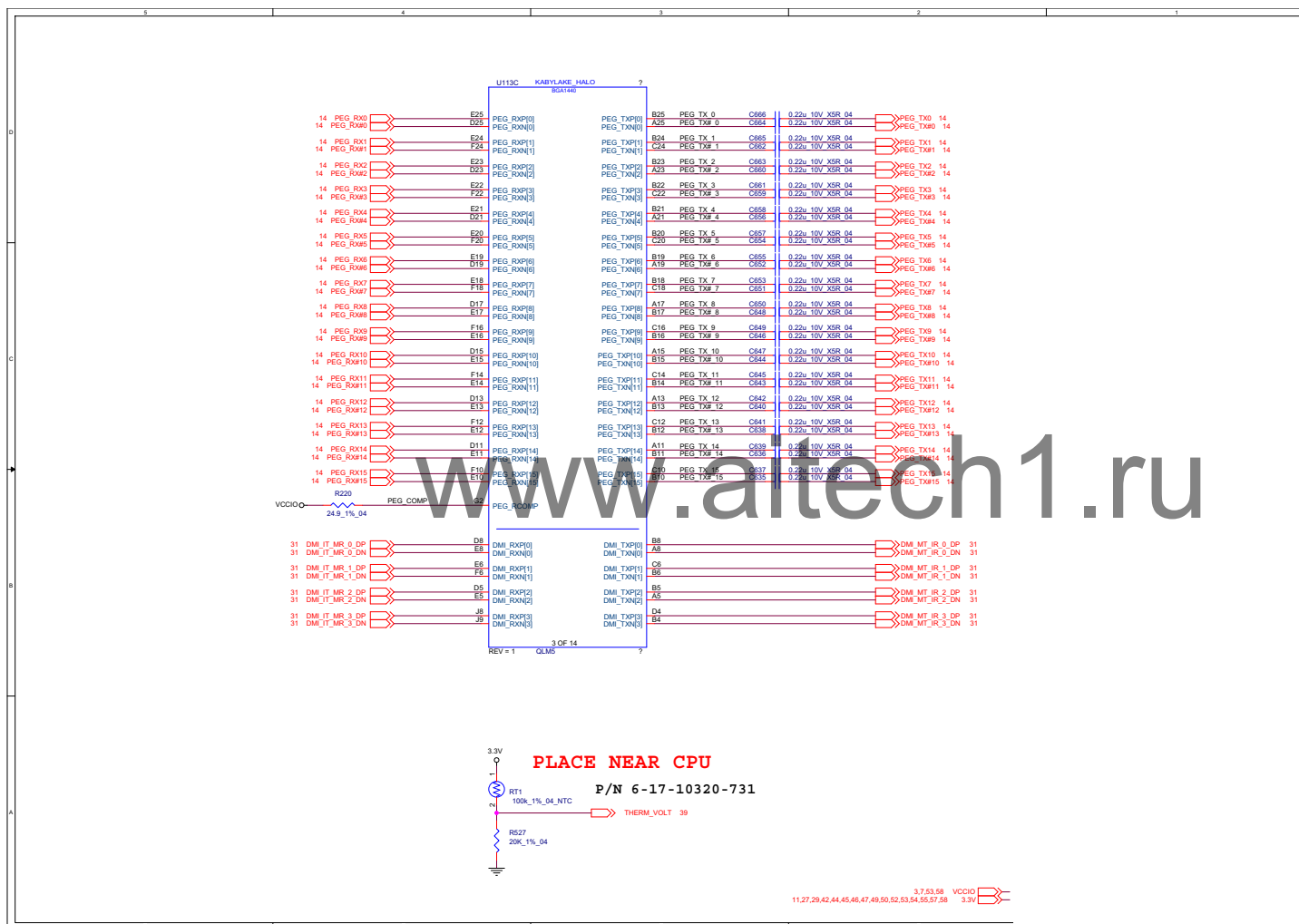
The schematic diagrams in this chapter are based upon version 6-7P-P65P9-002. If your mainboard (or other boards) are a later version, please check with the Service Center for updated diagrams (if required).

# System Block Diagram

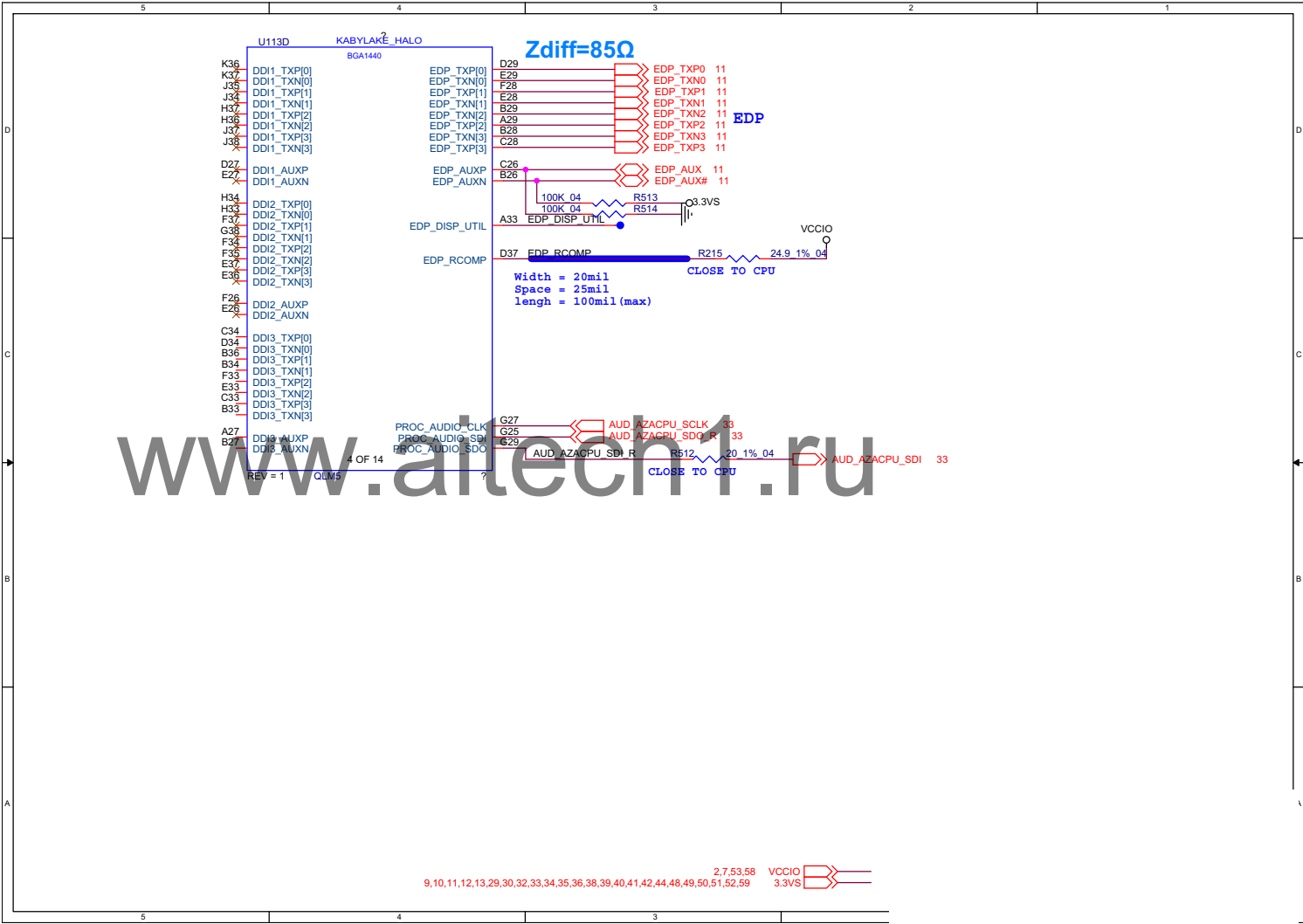


Sheet 1 of 74  
System Block  
Diagram

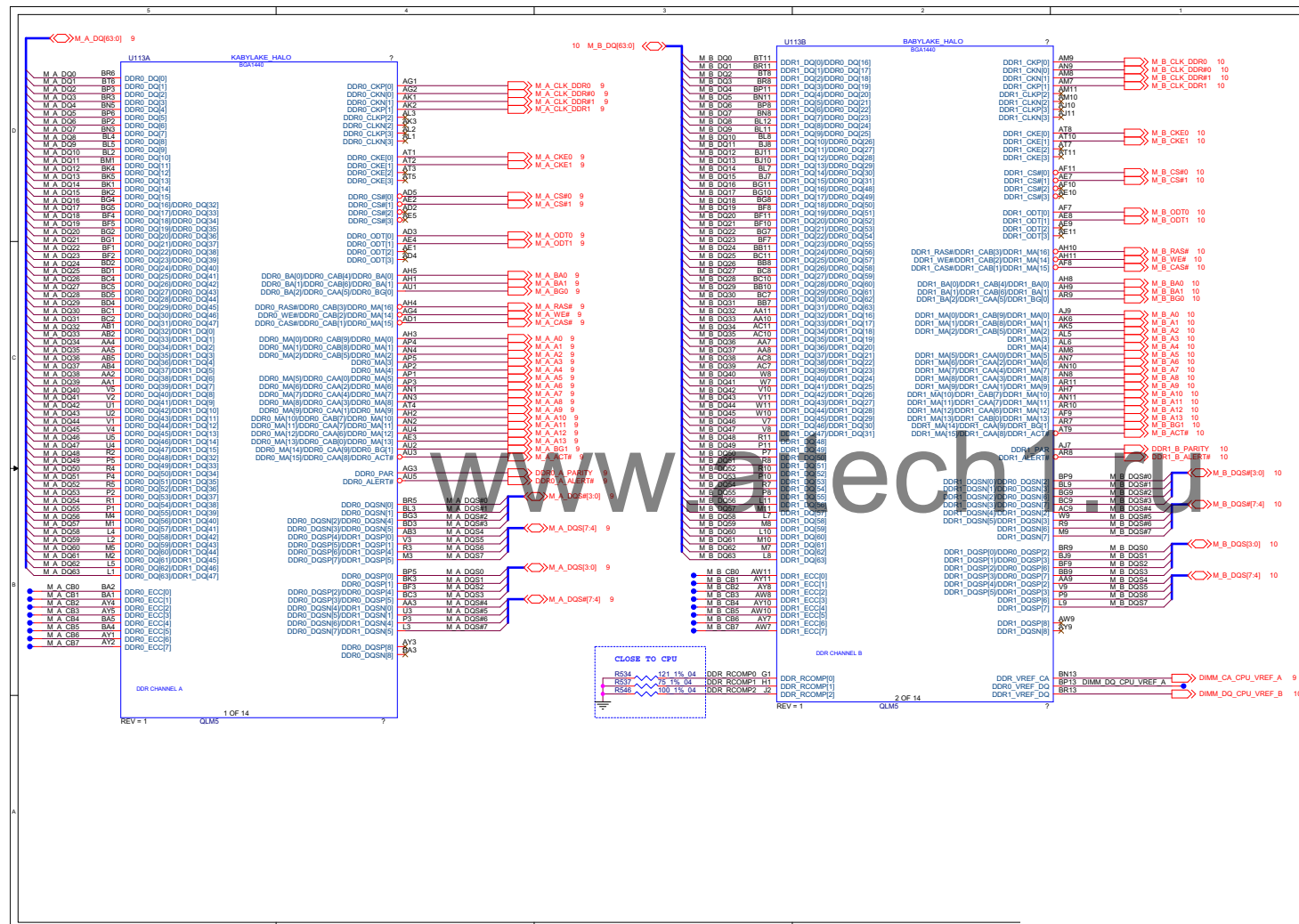
## Processor 1/7

Sheet 2 of 74  
Processor 1/7

Processor 2/7



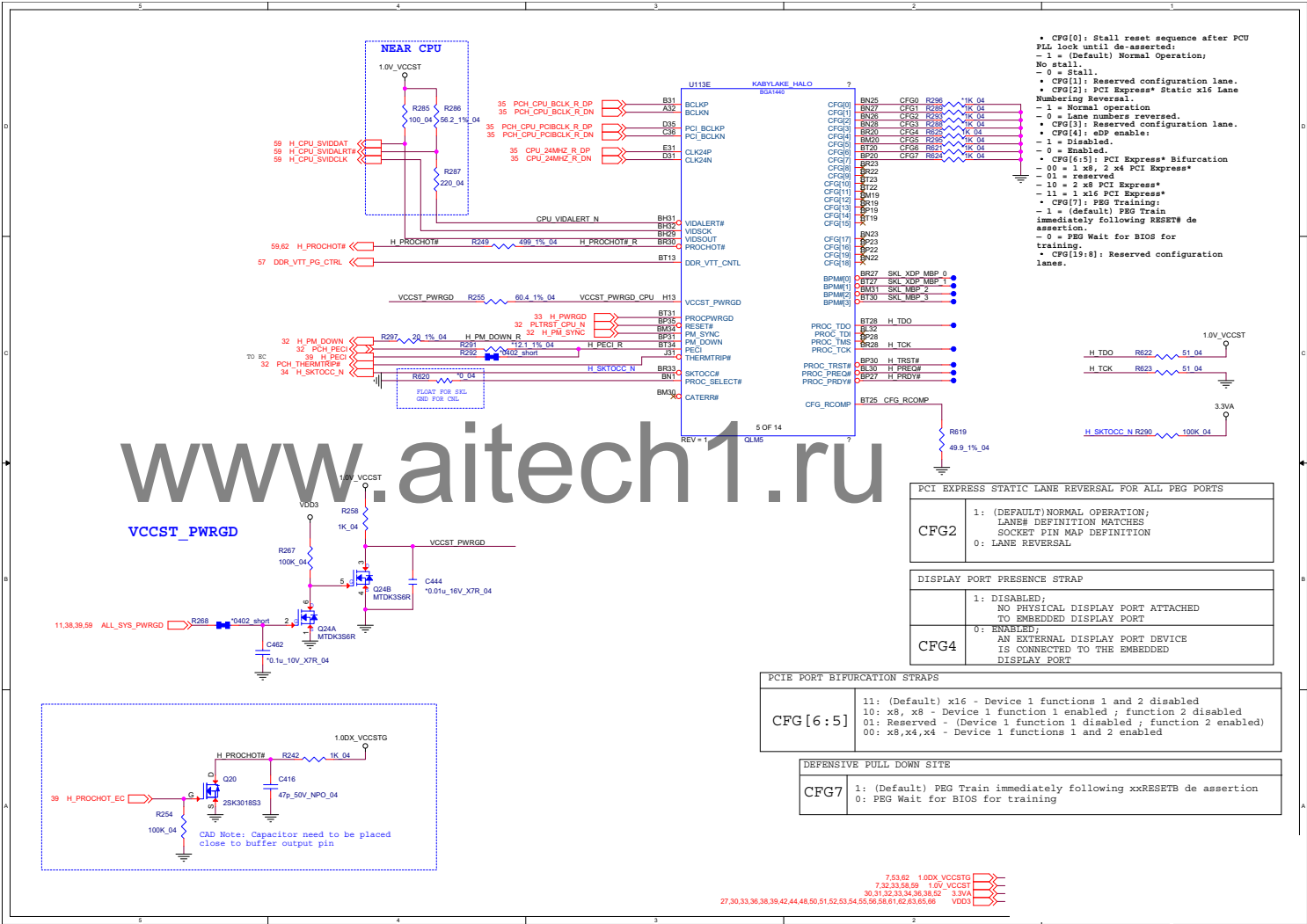
## B.Schematic Diagrams



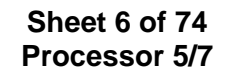
Schematic Diagrams

Processor 4/7

Sheet 5 of 74  
Processor 4/7



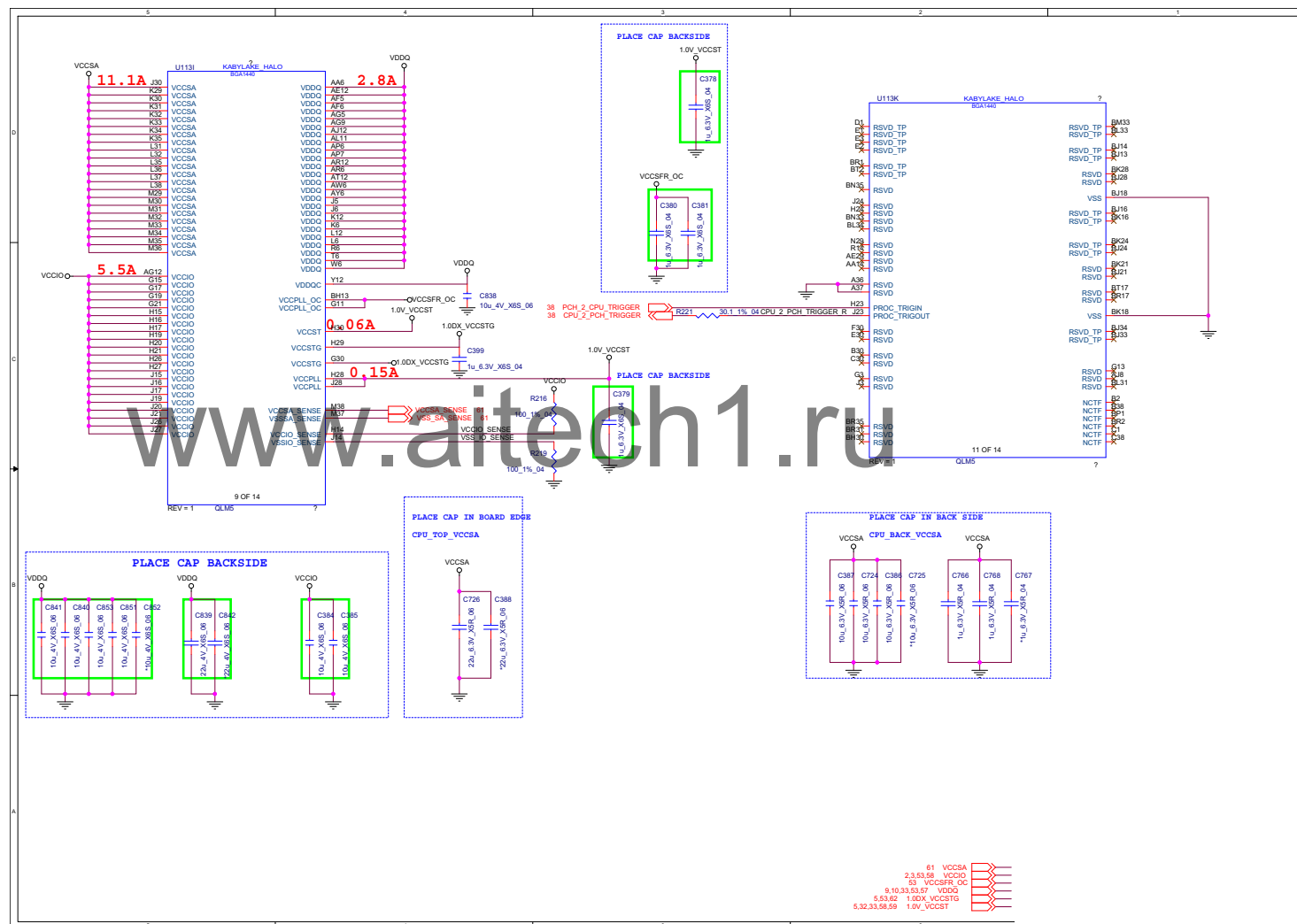
**Processor 5/7 B - 7**



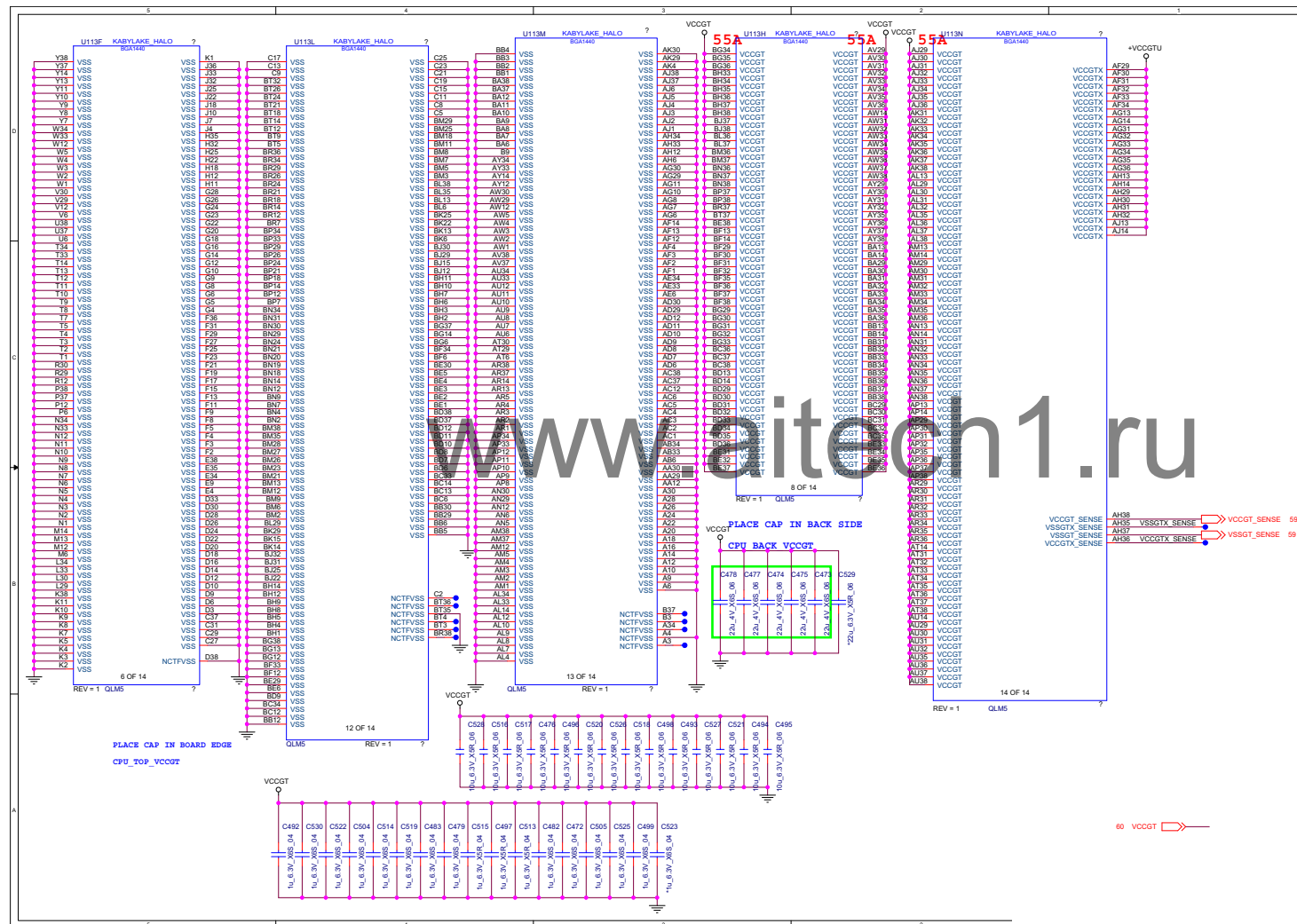
## Processor 6/7

## B. Schematic Diagrams

Sheet 7 of 74  
Processor 6/

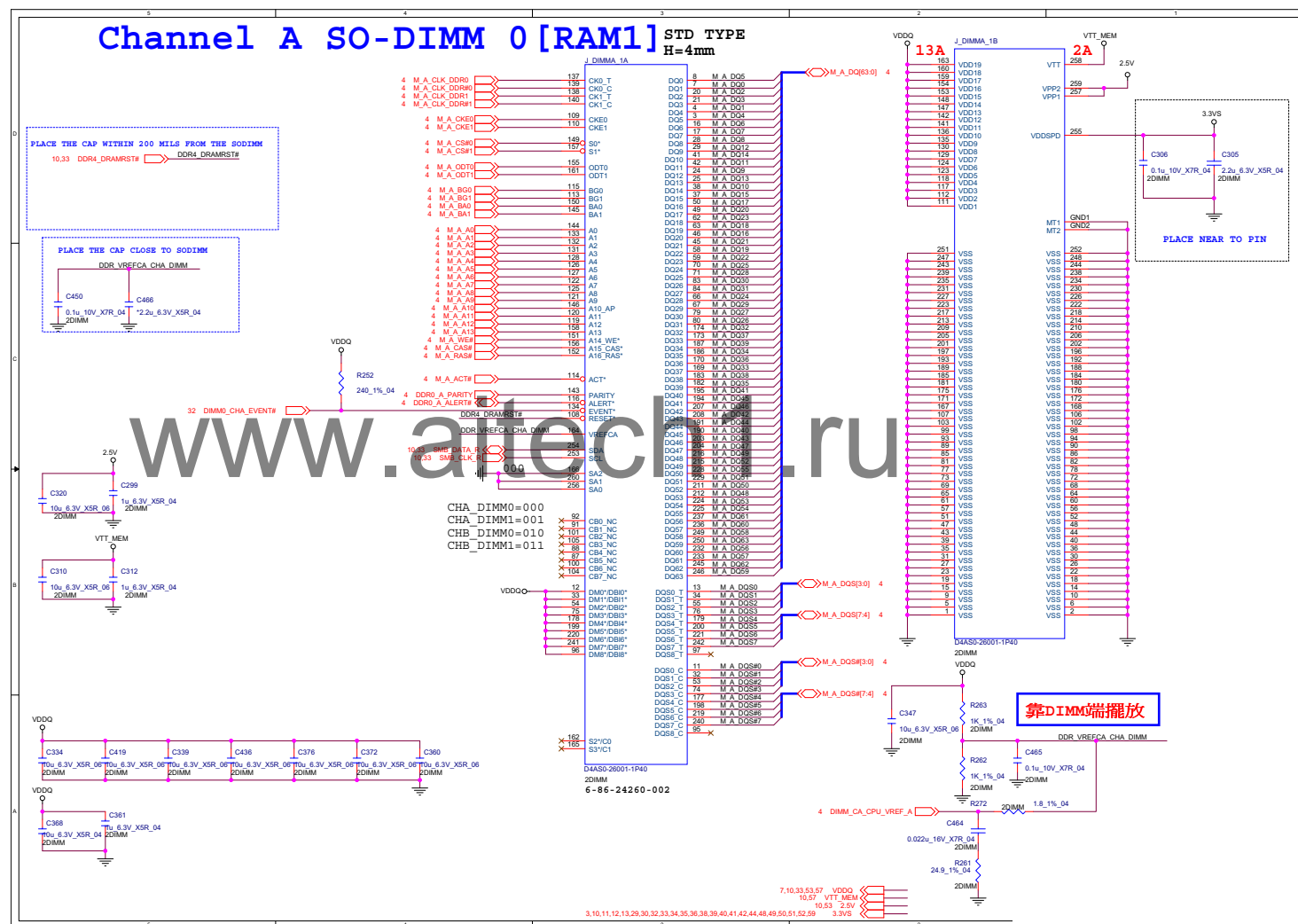


**Processor 7/7 B - 9**



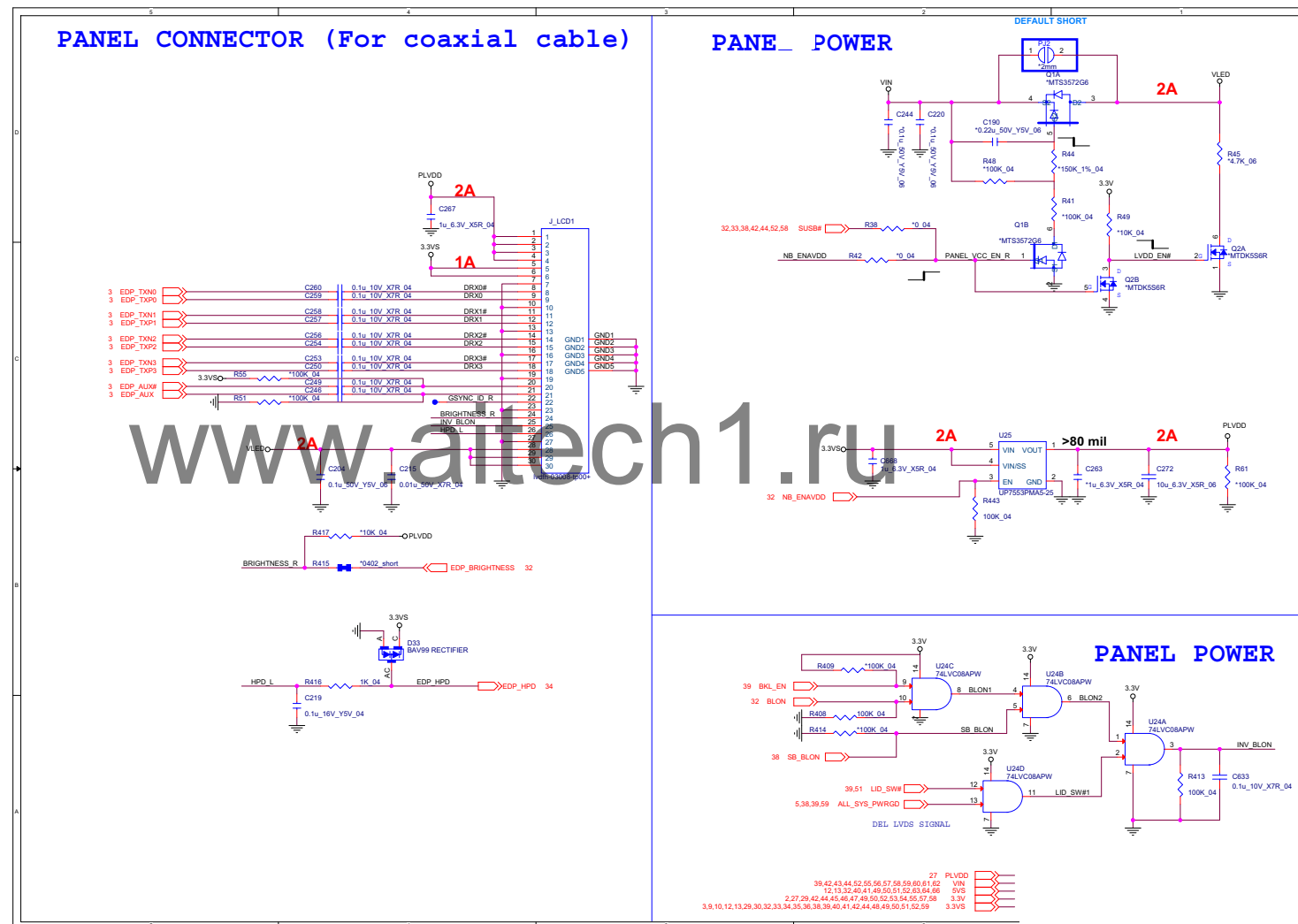
## DDR4 CHA SO-DIMM\_0

Sheet 9 of 74  
DDR4 CHA SO-  
DIMM\_0

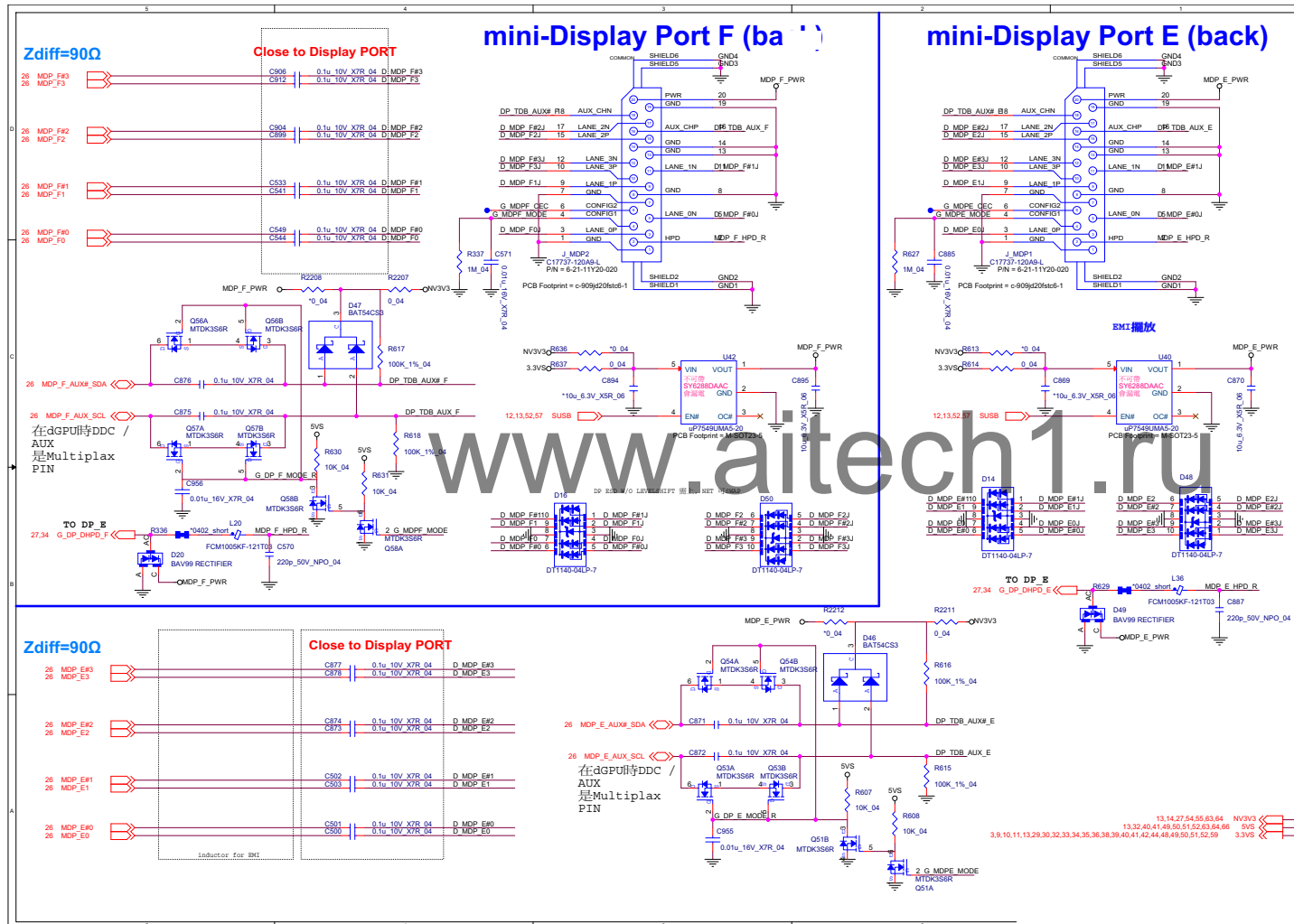


## B.Schematic Diagrams

**Sheet 11 of 74**  
**Panel, Inverter**



## Mini DP Port

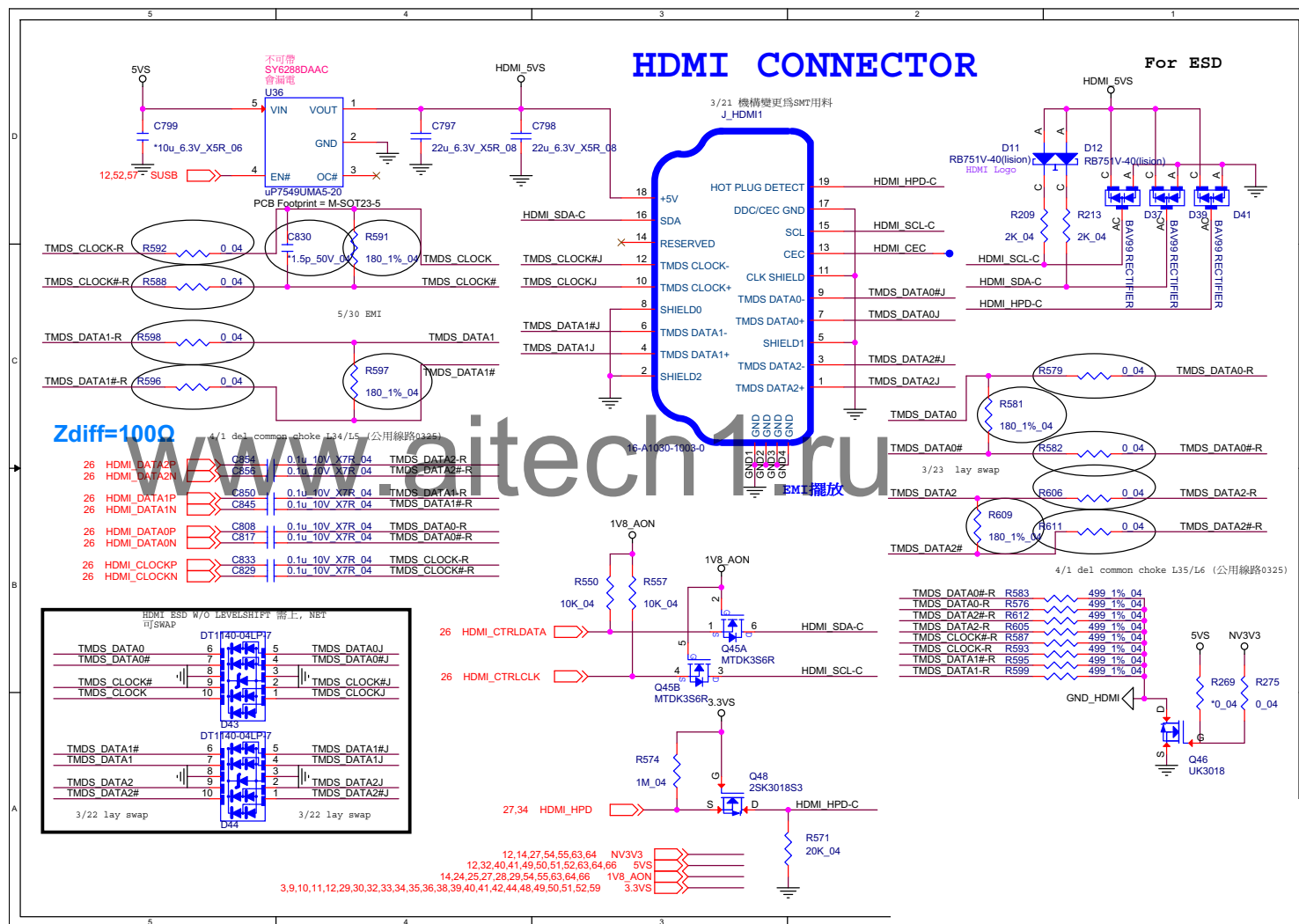


Sheet 12 of 74  
Mini DP Port

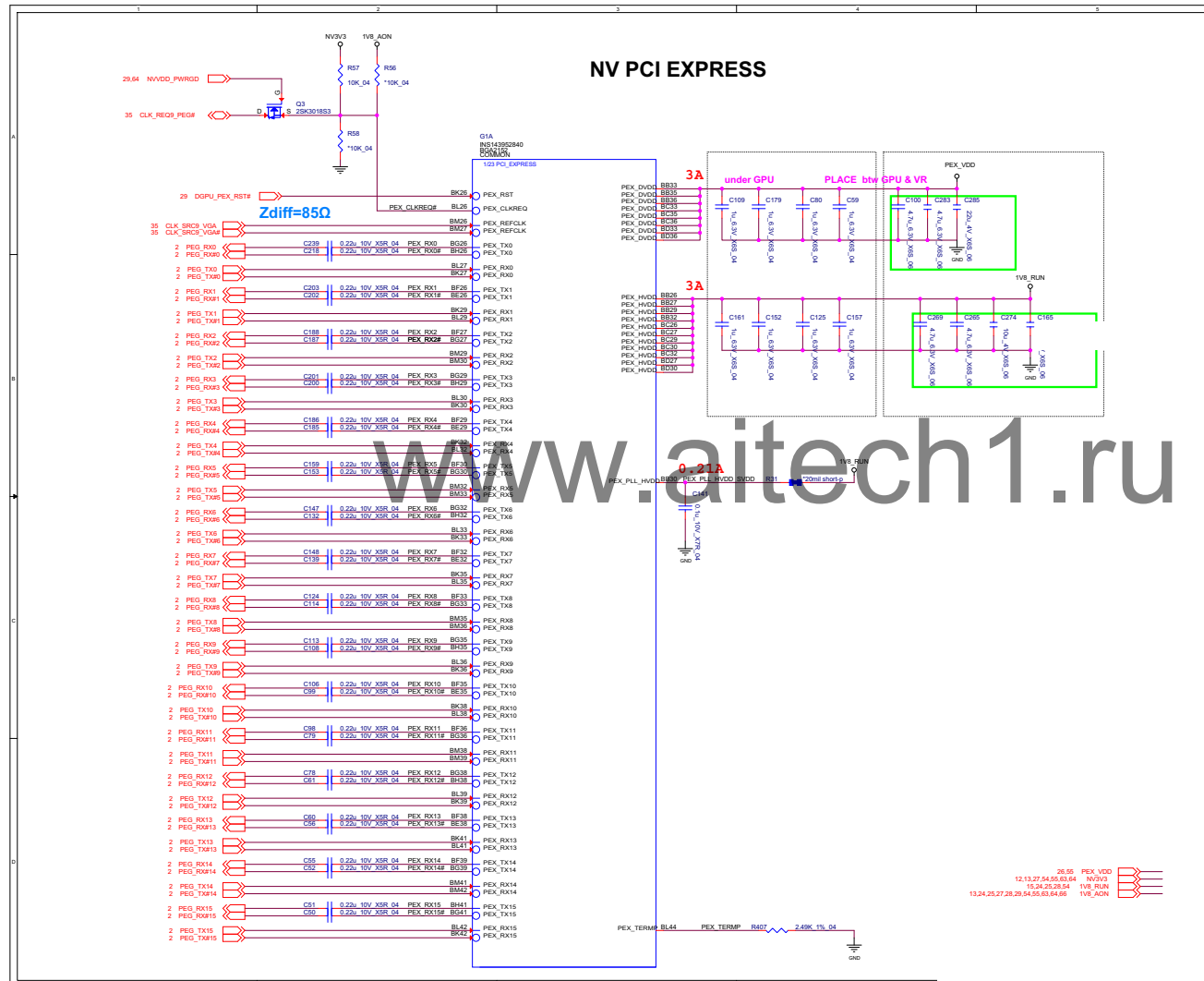
## HDMI Connector

## B. Schematic Diagrams

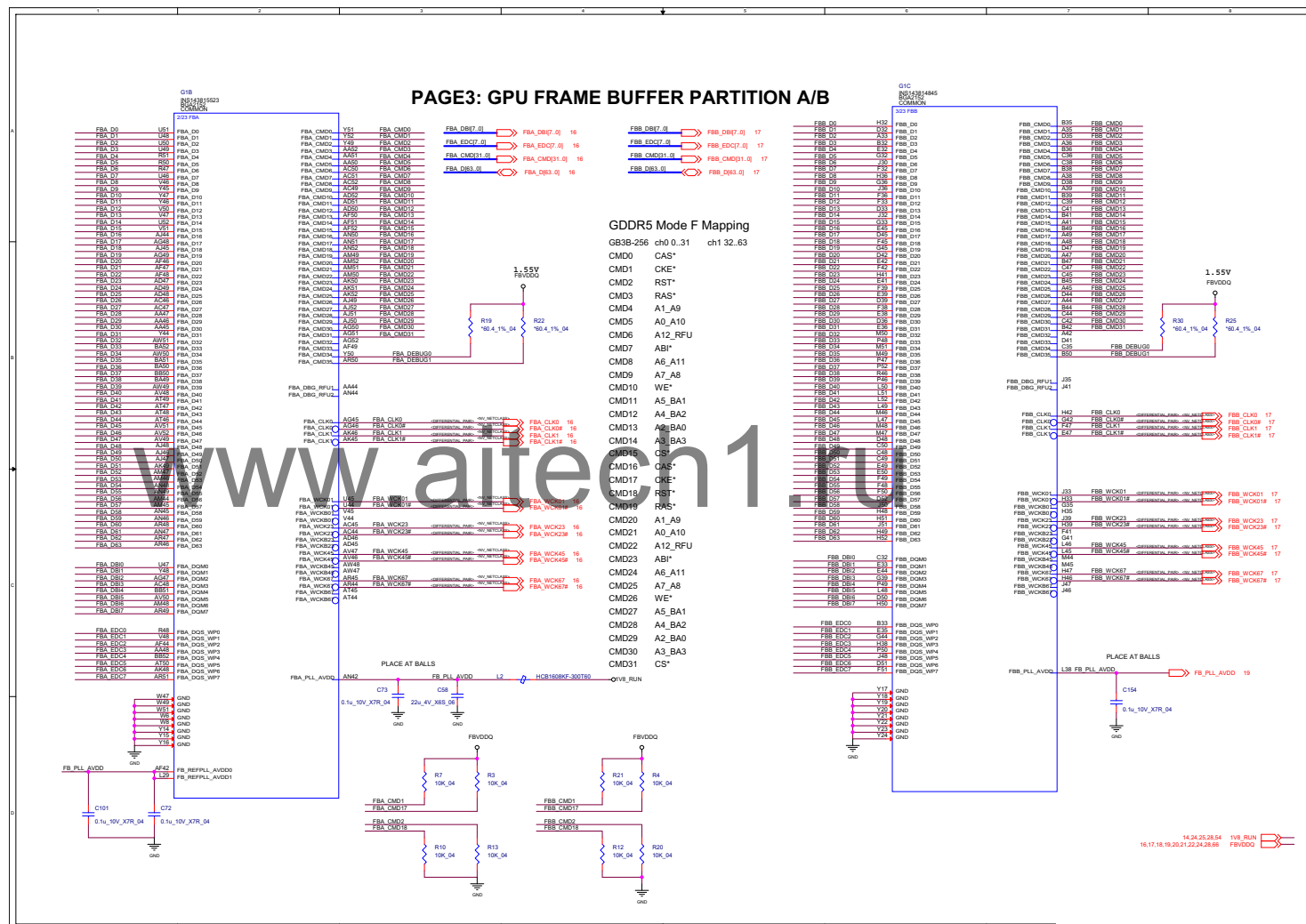
Sheet 13 of 74  
HDMI Connector



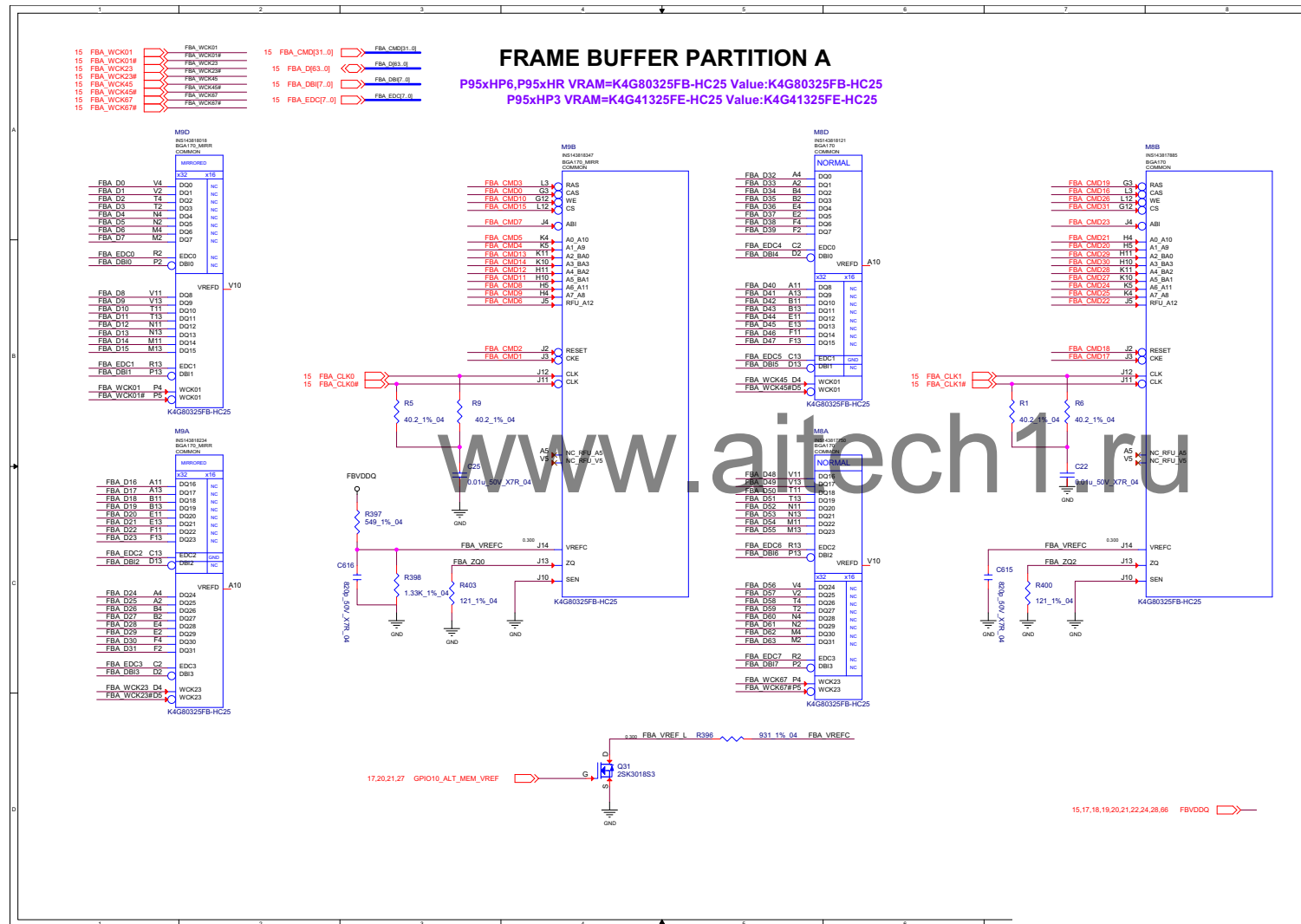
## VGA PCI Express B - 15



## B - 16 GPU Frame Buffer Partition



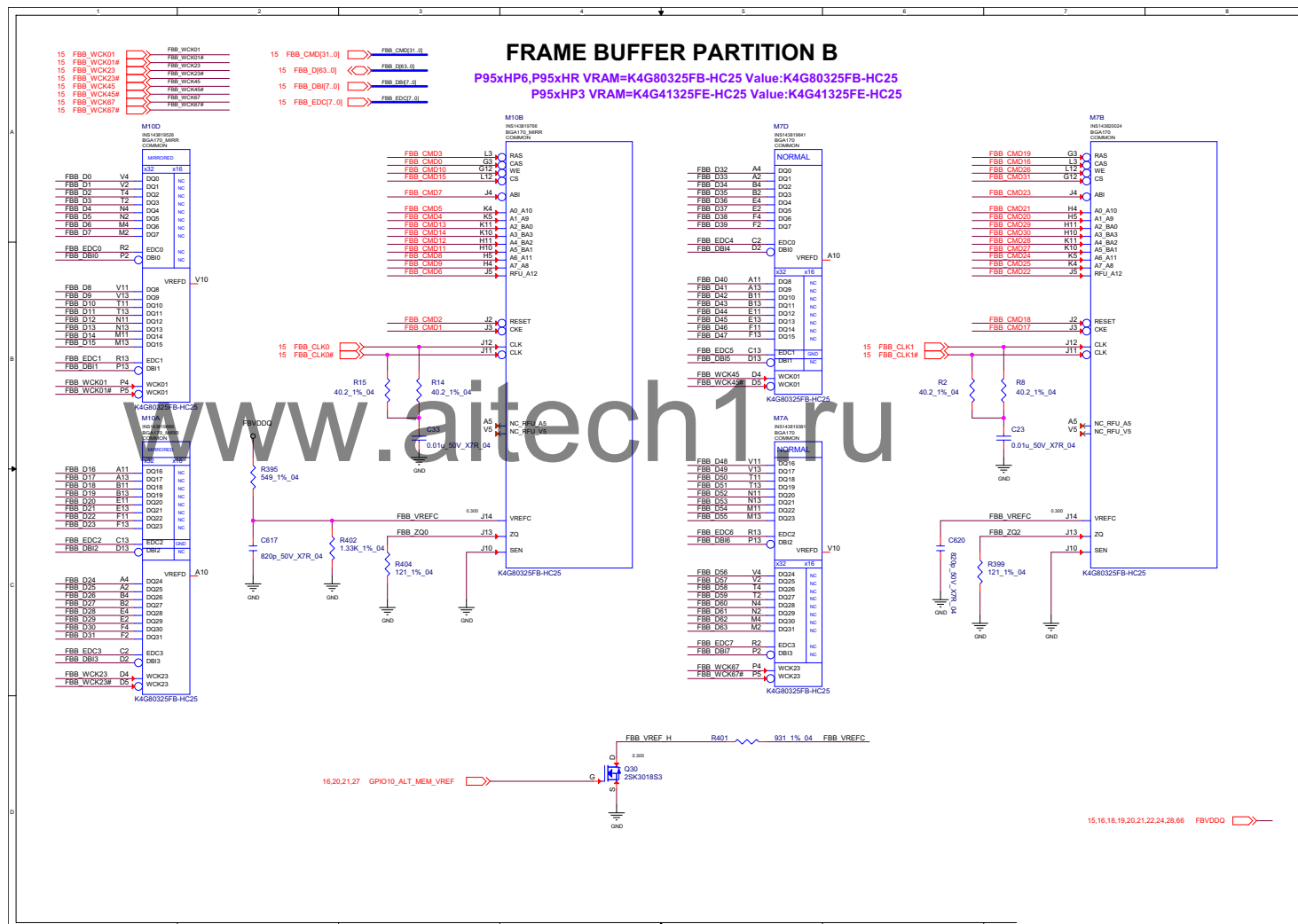
# Frame Buffer Partition A



Sheet 16 of 74  
Frame Buffer  
Partition A

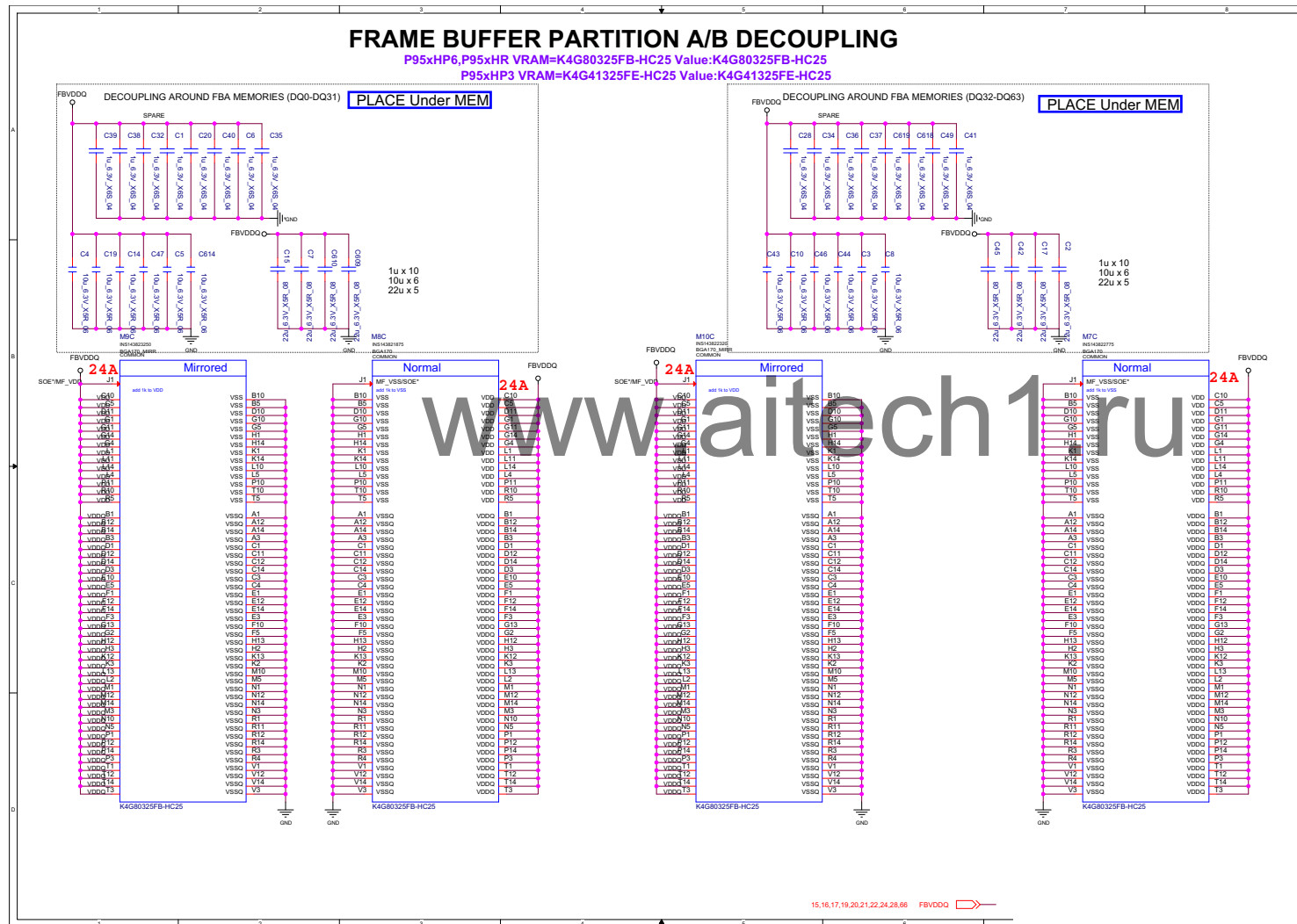
## Frame Buffer Partition B

## B. Schematic Diagrams



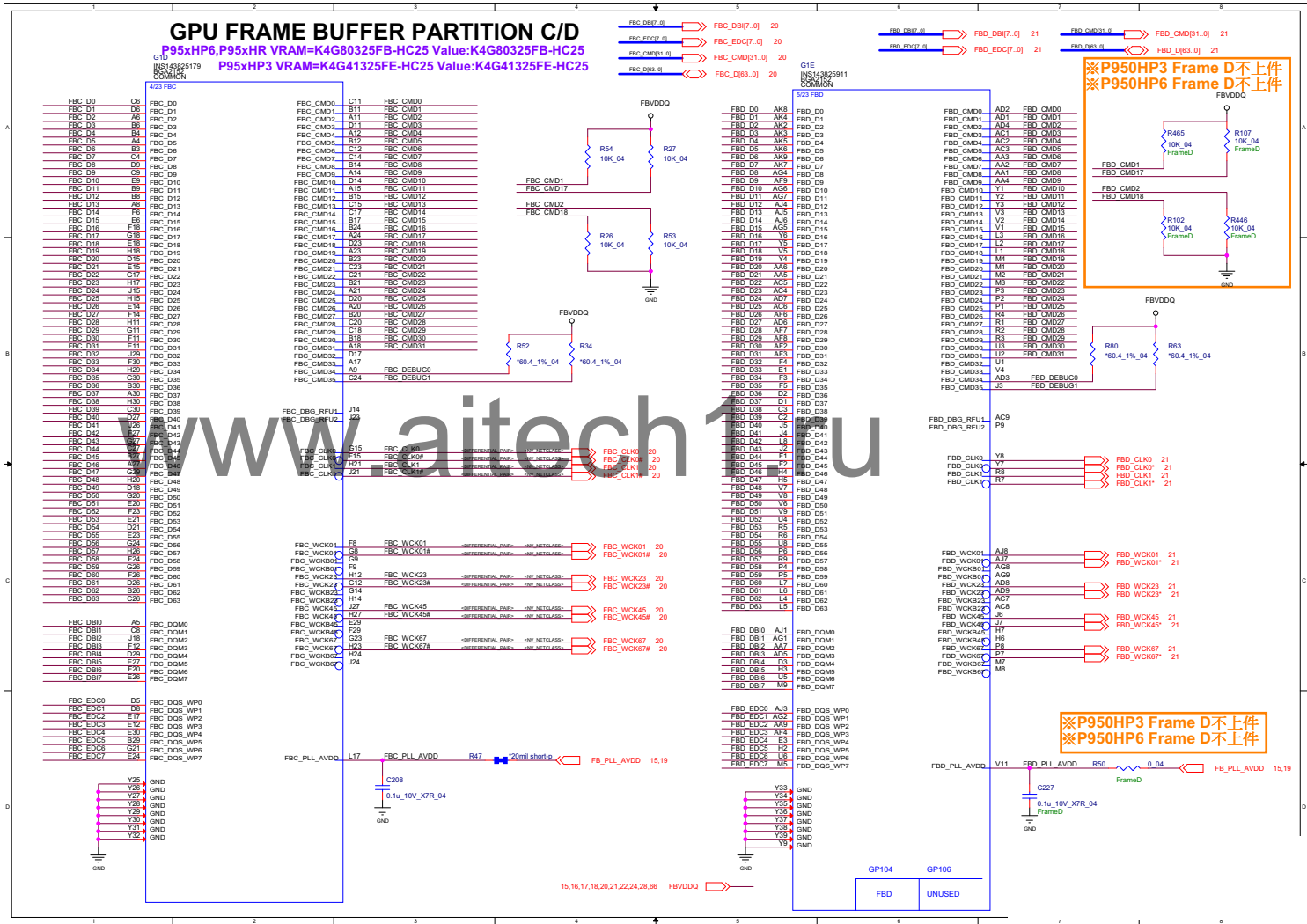
## Frame Buffer Partition A\_B

Sheet 18 of 74  
Frame Buffer  
Partition A\_B

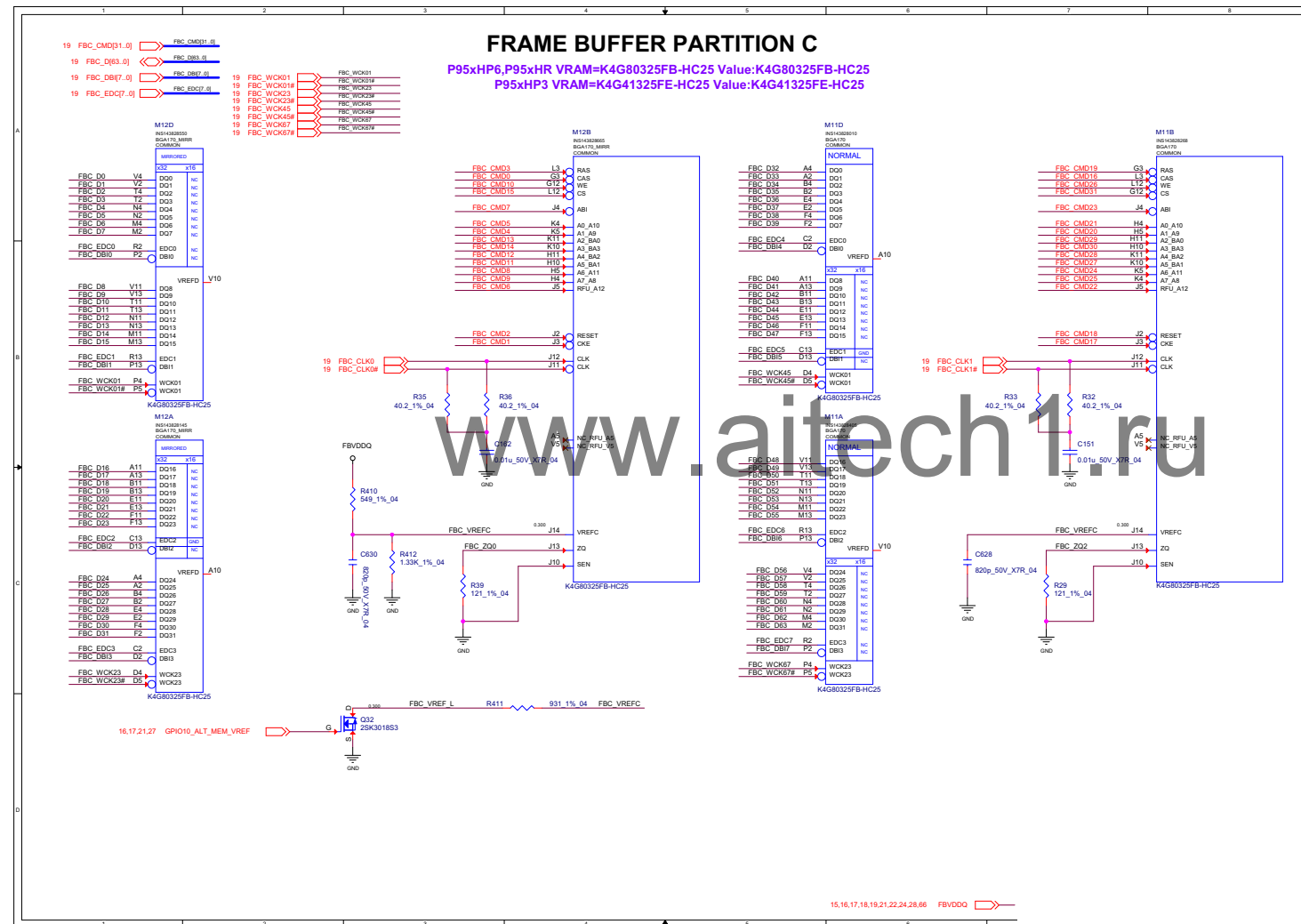


# GPU Frame Buffer Partition

Sheet 19 of 74  
GPU Frame Buffer  
Partition

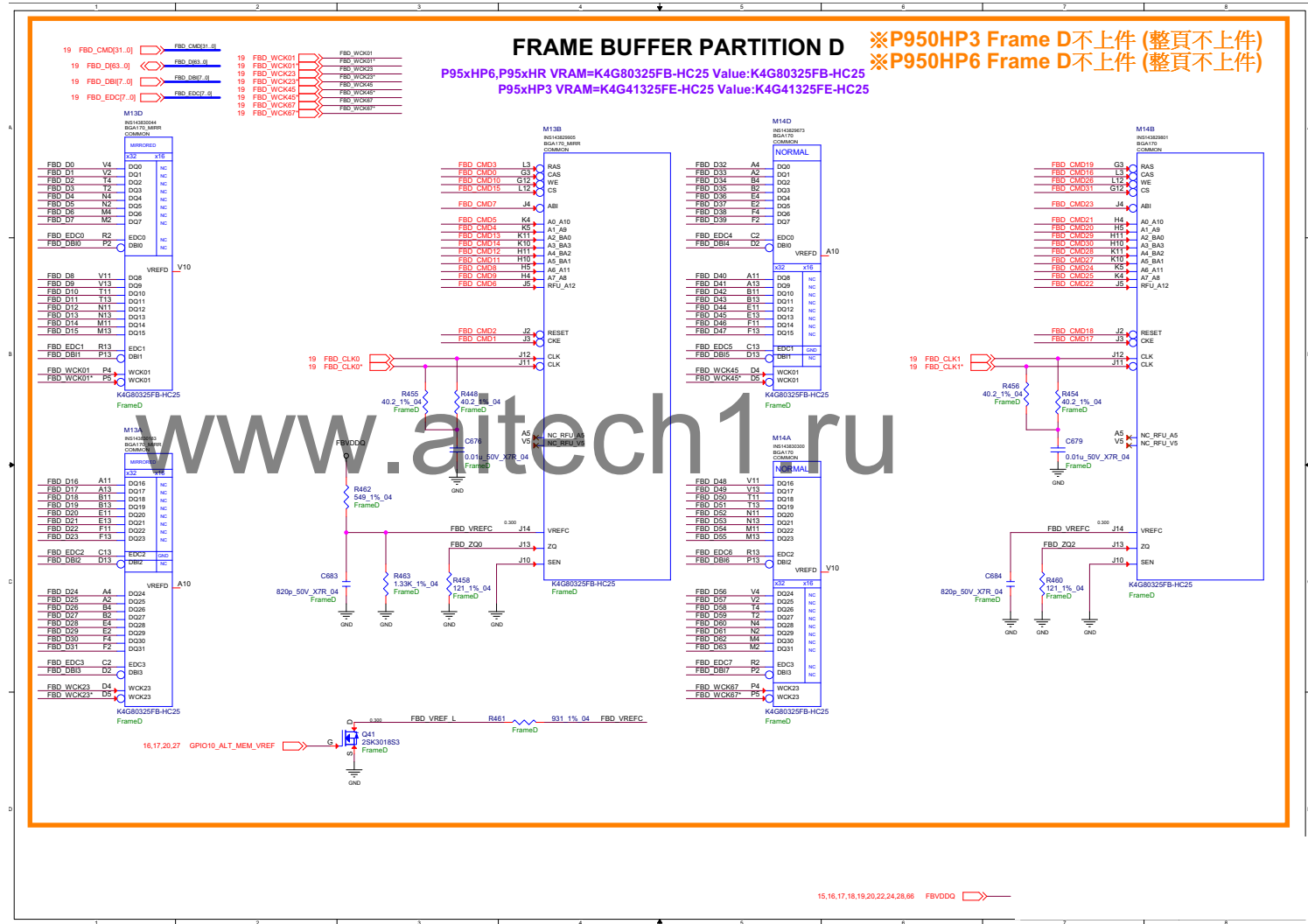


# Frame Buffer Partition C



# Frame Buffer Partition D

Sheet 21 of 74  
Frame Buffer  
Partition D



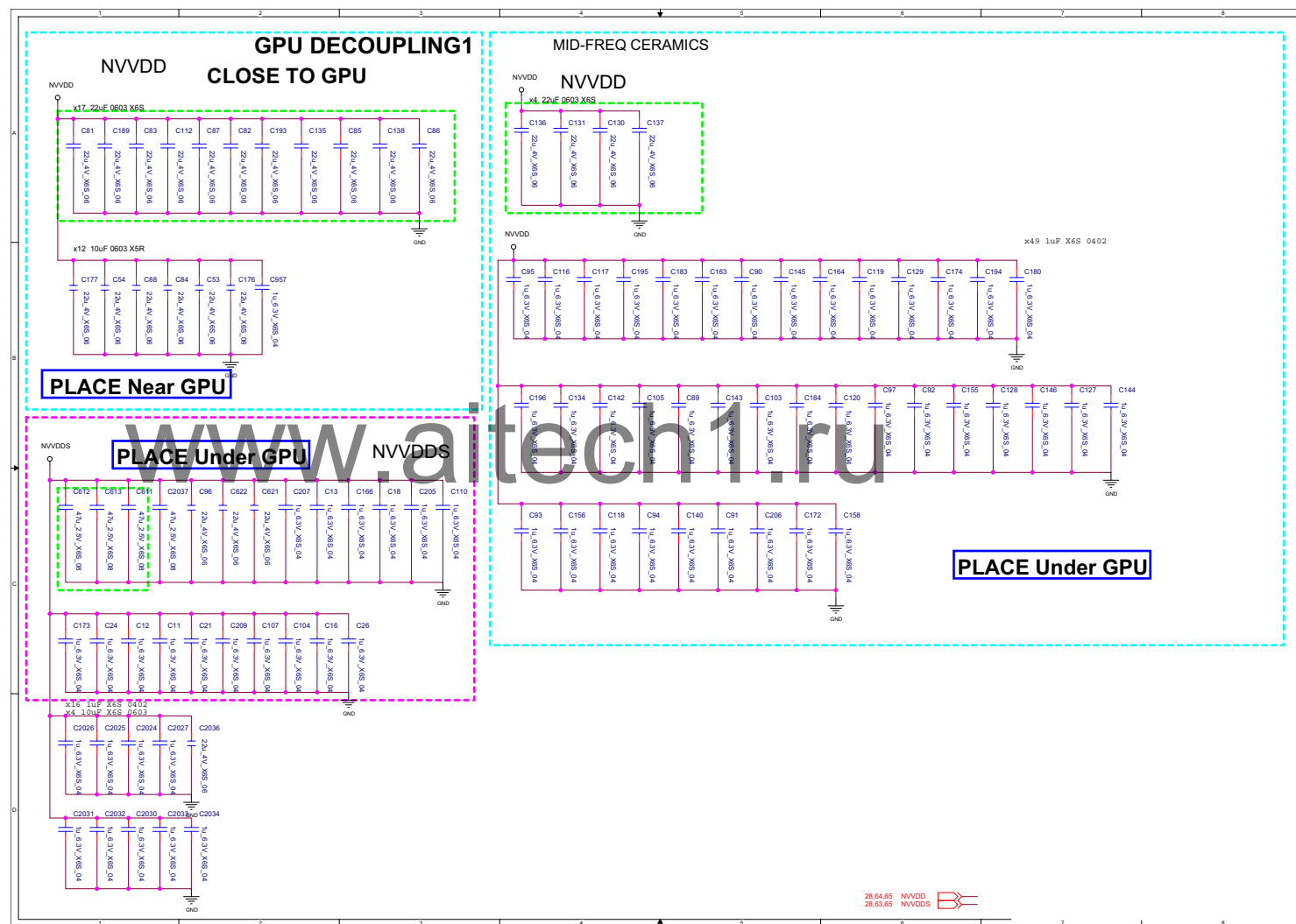
Sheet 22 of 74  
Frame Buffer  
Partition C\_D



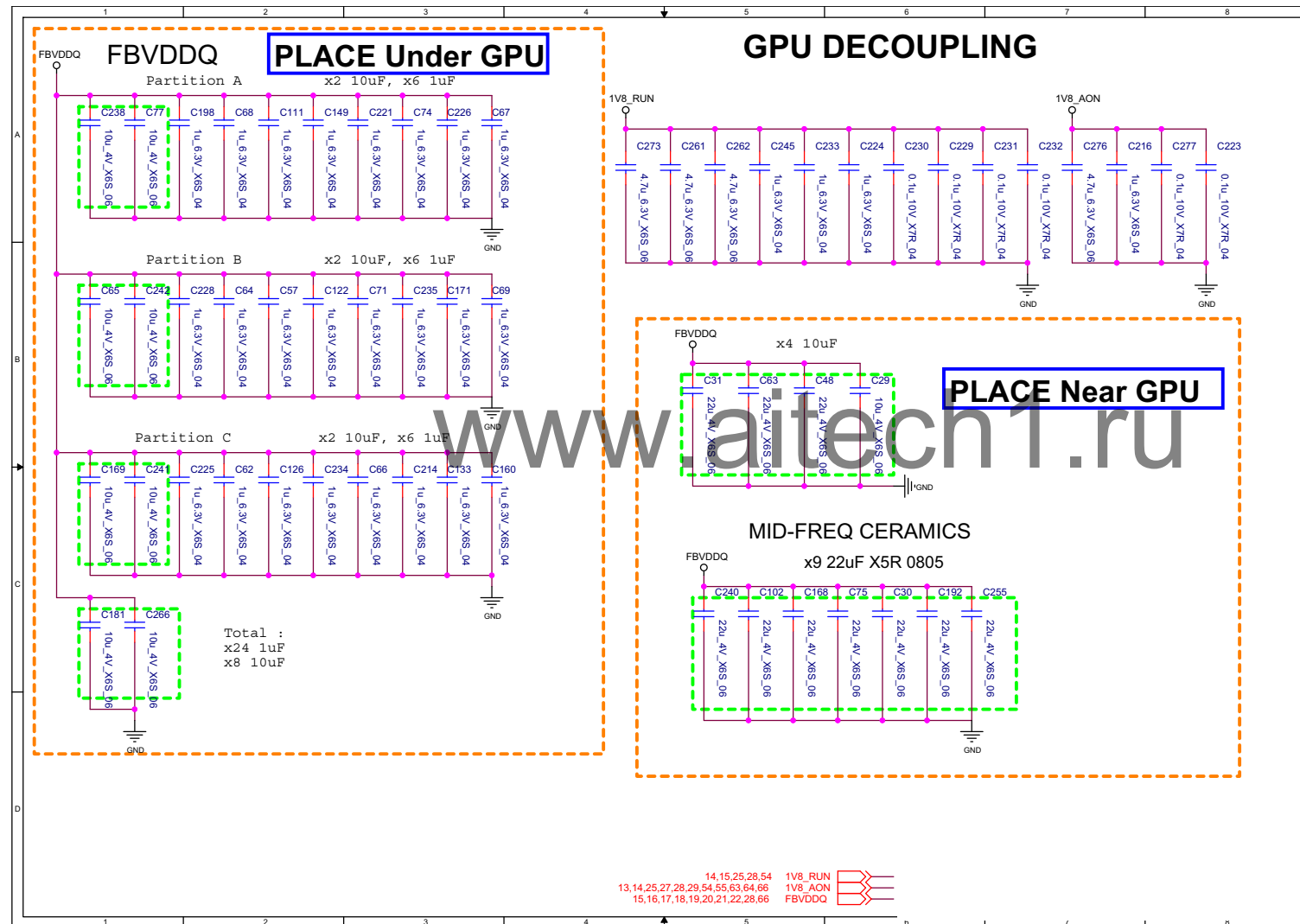
## Schematic Diagrams

## GPU Decoupling 1

Sheet 23 of 74  
GPU Decoupling 1



## GPU Decoupling 2

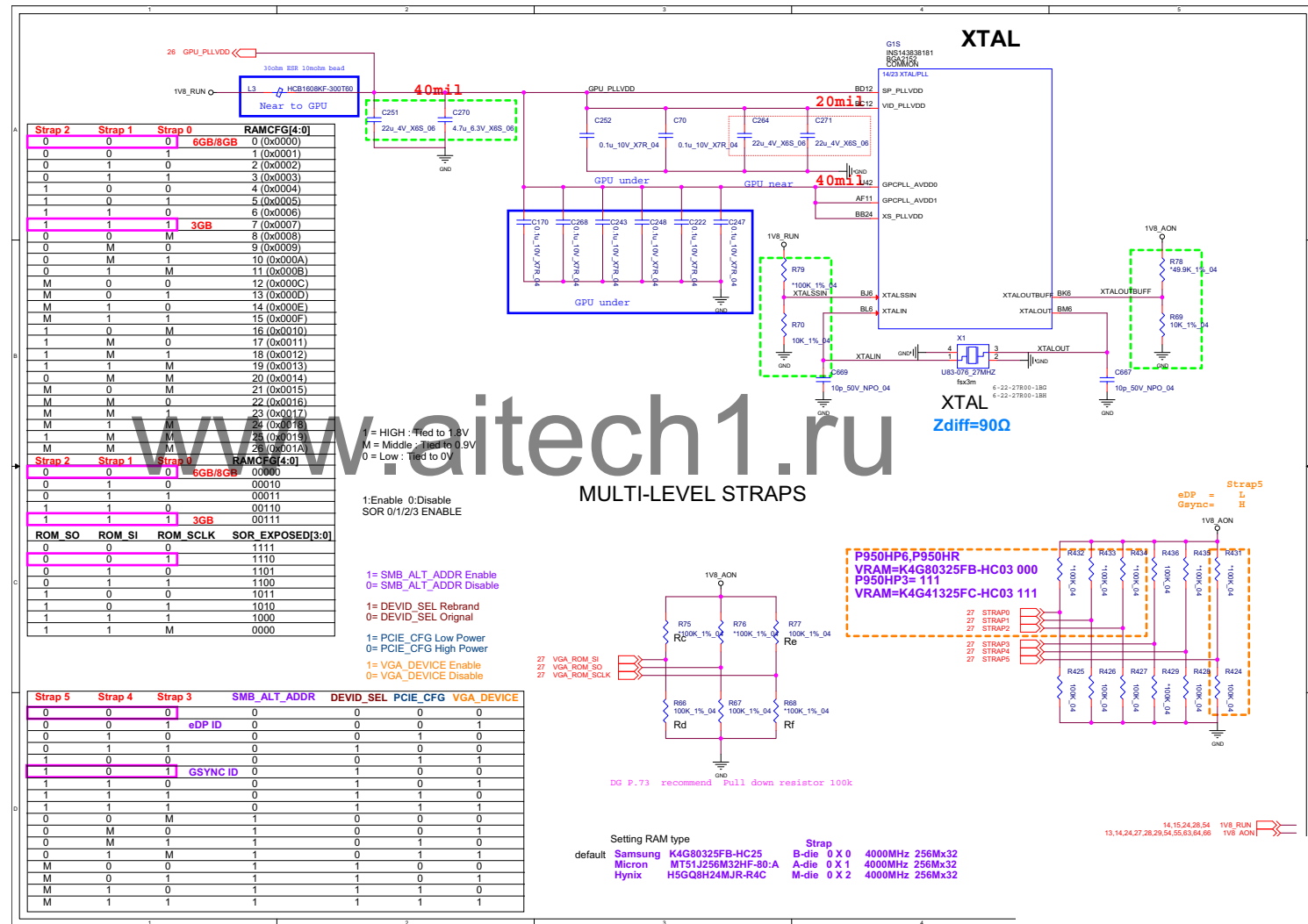


Sheet 24 of 74  
GPU Decoupling 2

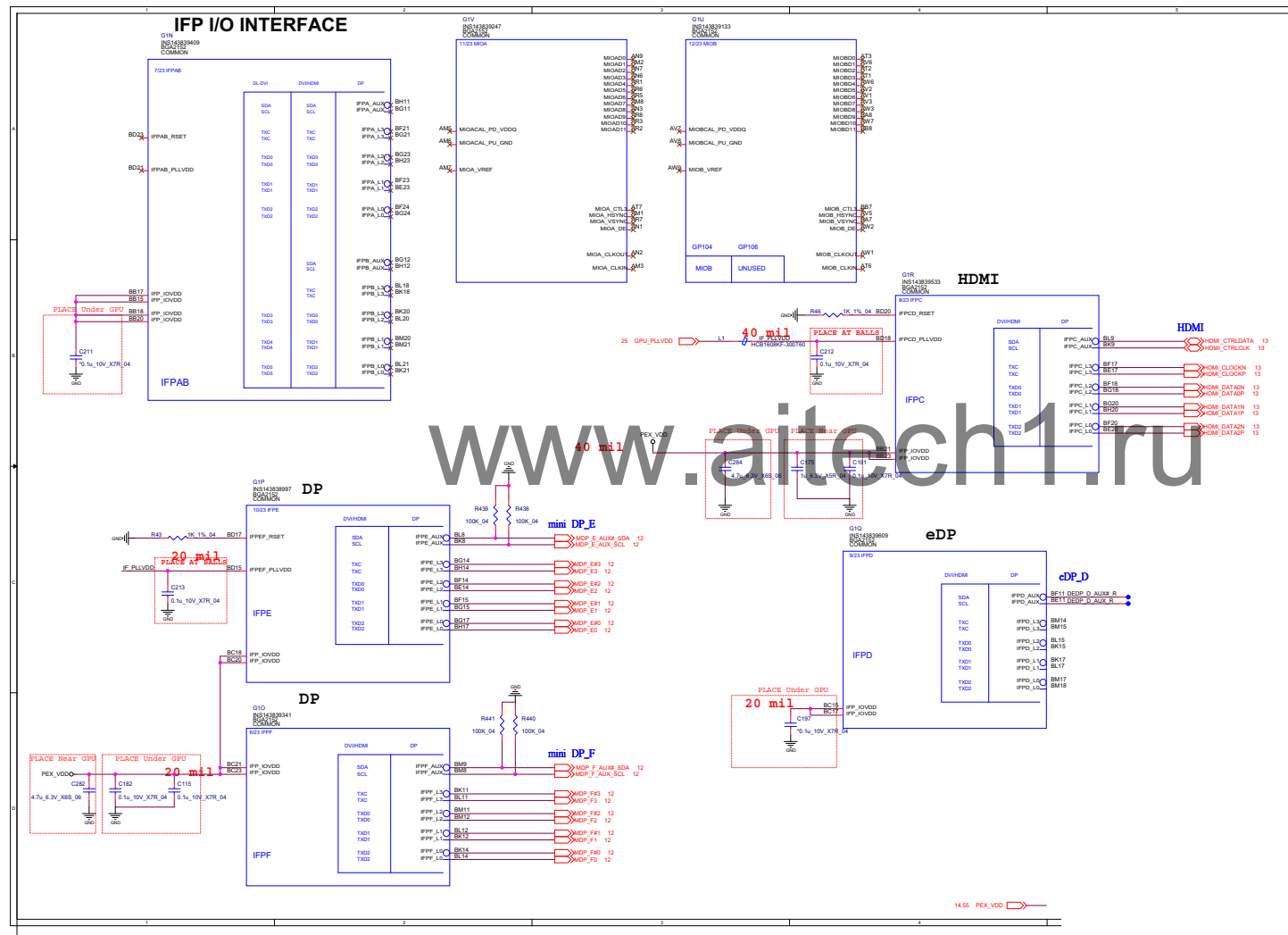
## Schematic Diagrams

## Straps and XTAL

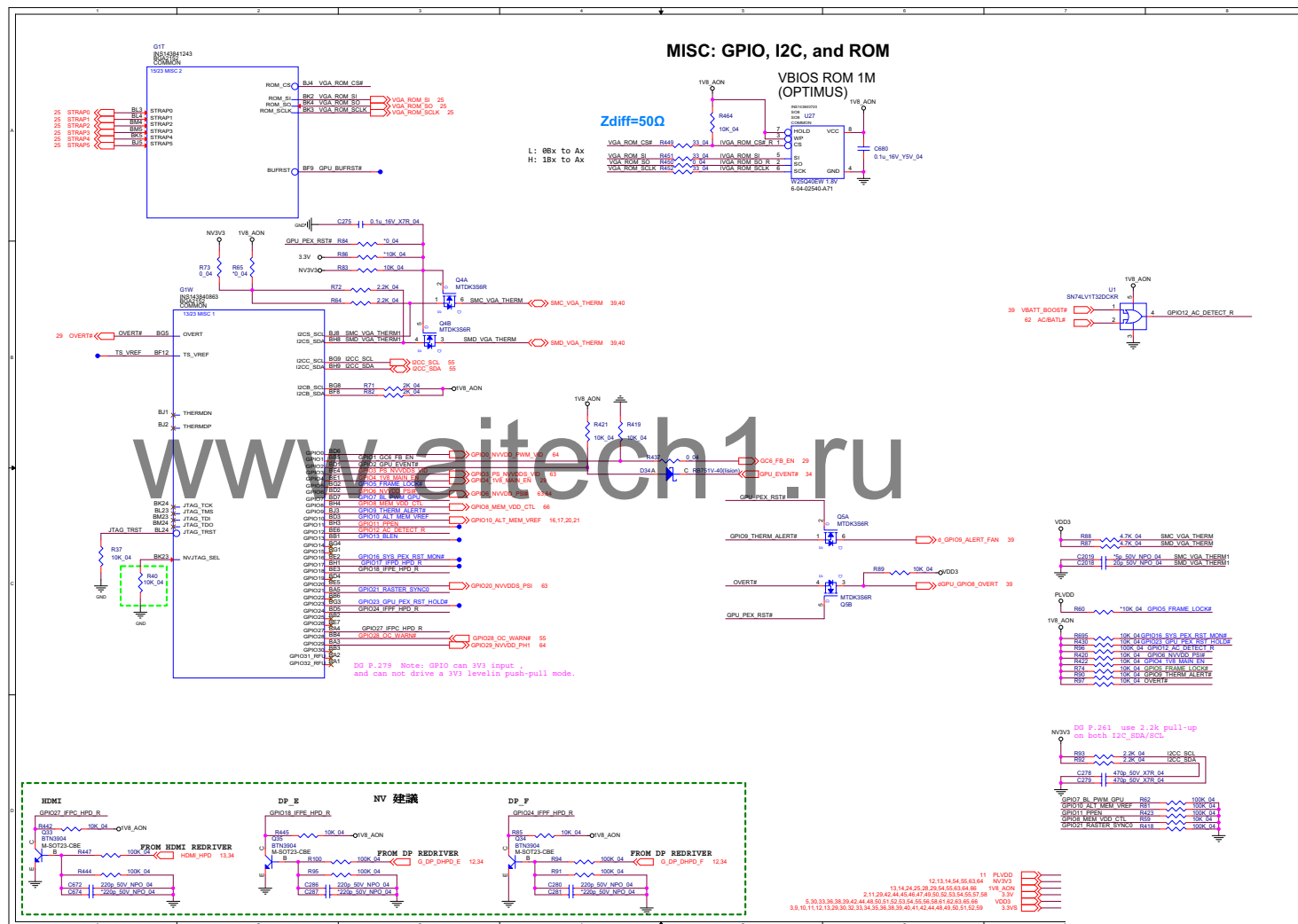
Sheet 25 of 74  
Straps and XTAL

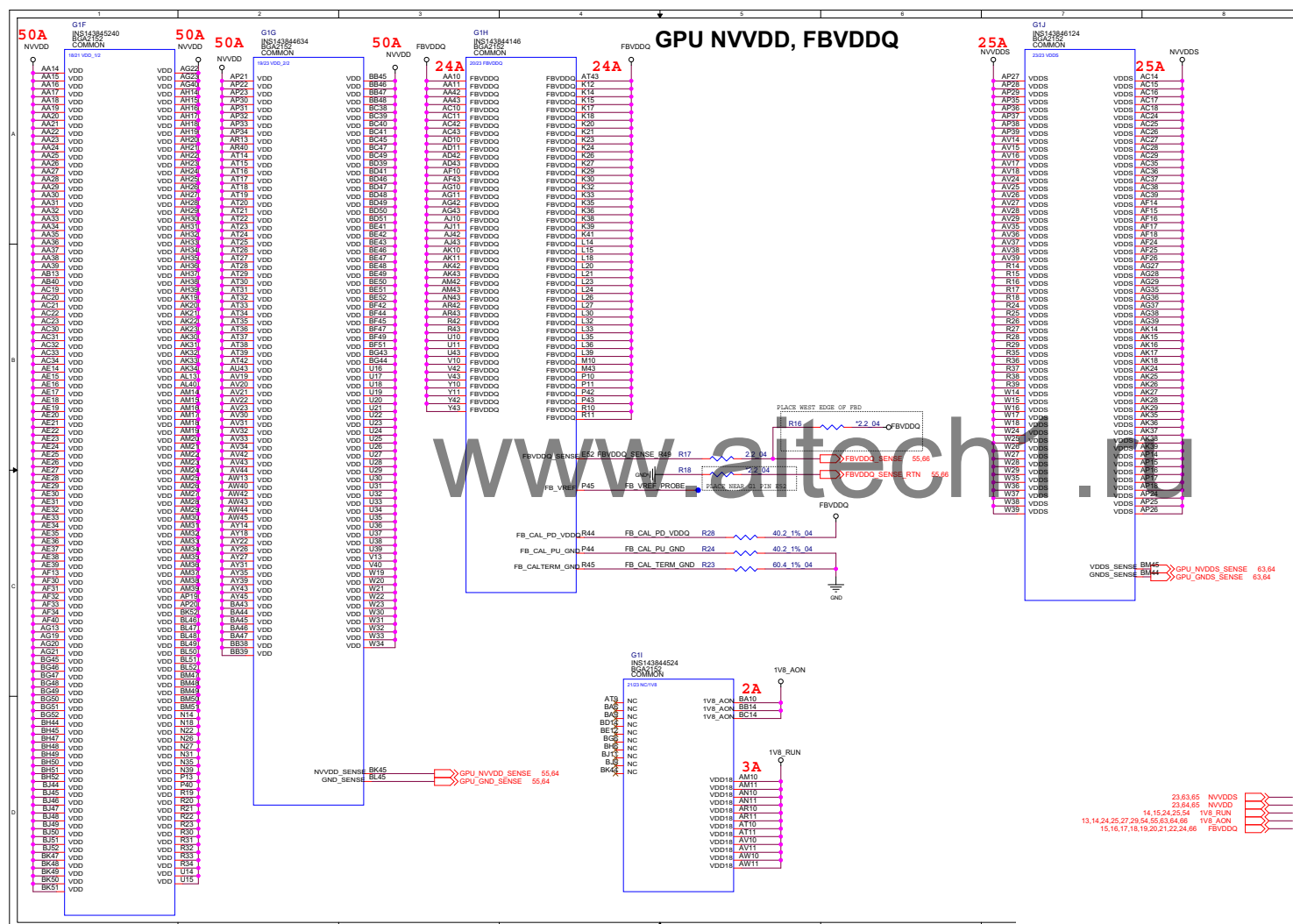


## IFP I/O Interface B - 27

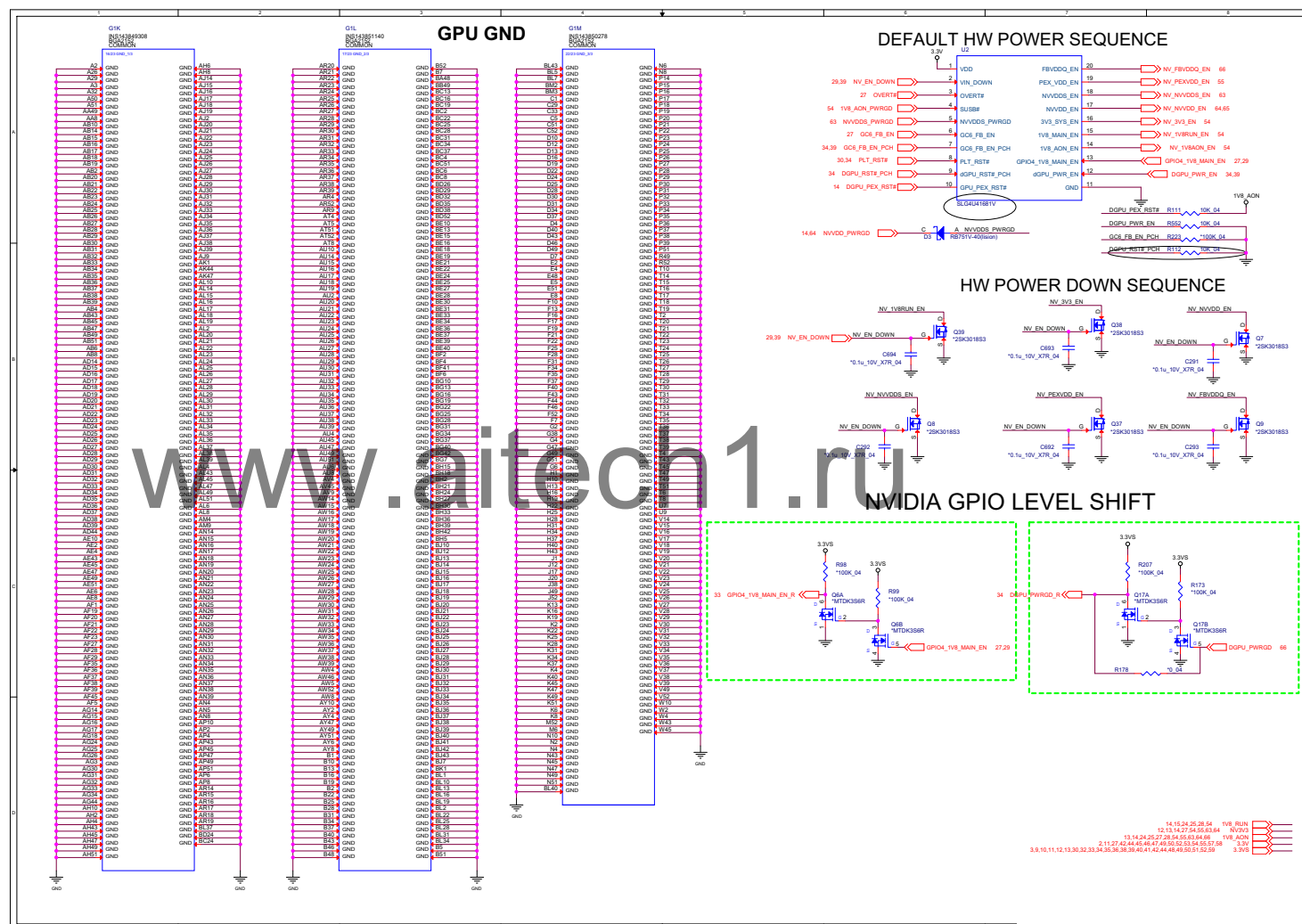


**Sheet 27 of 74**  
**Misc - GPIO, I2C**  
**and ROM**





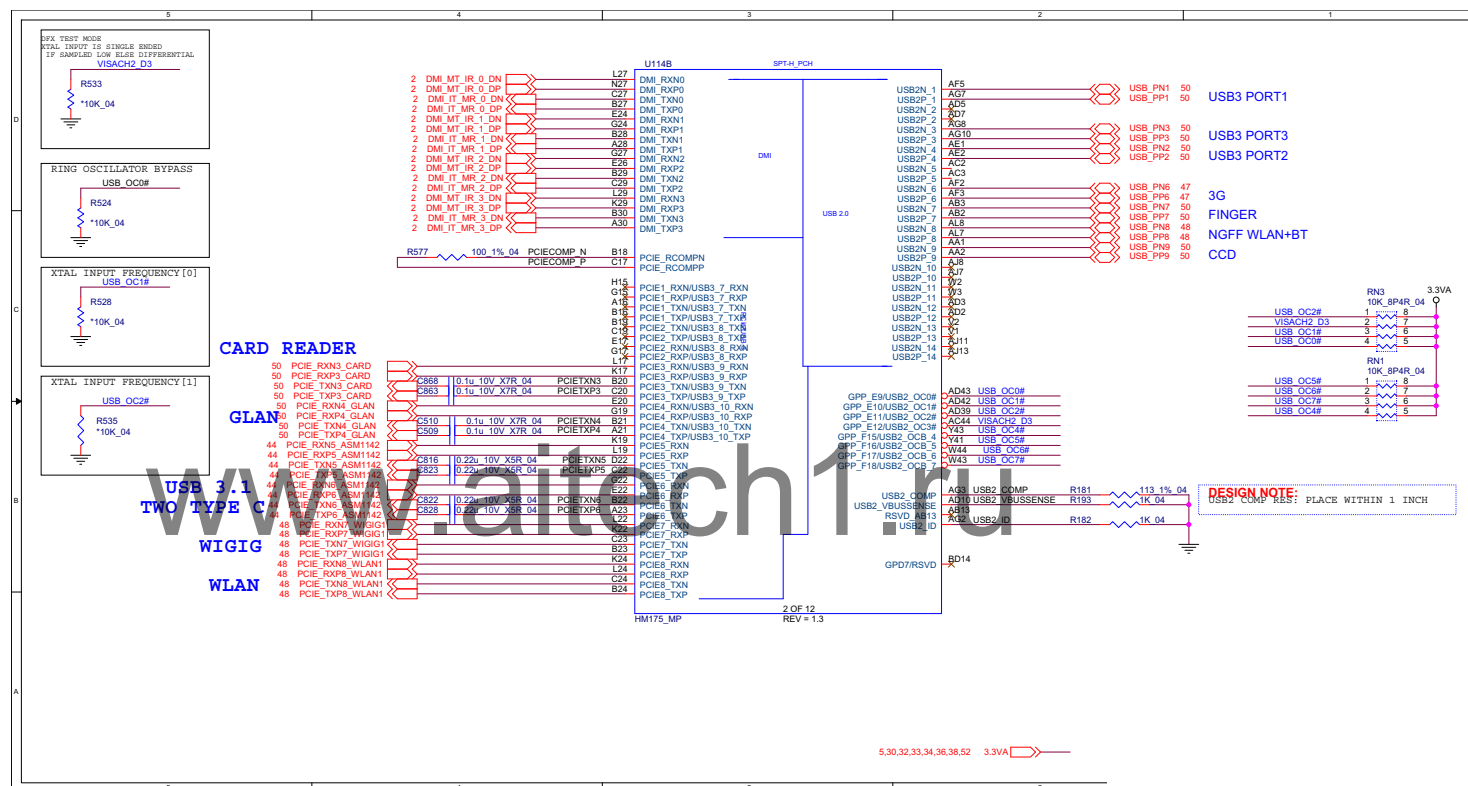
Sheet 29 of 74  
GPU GND &  
Sequence

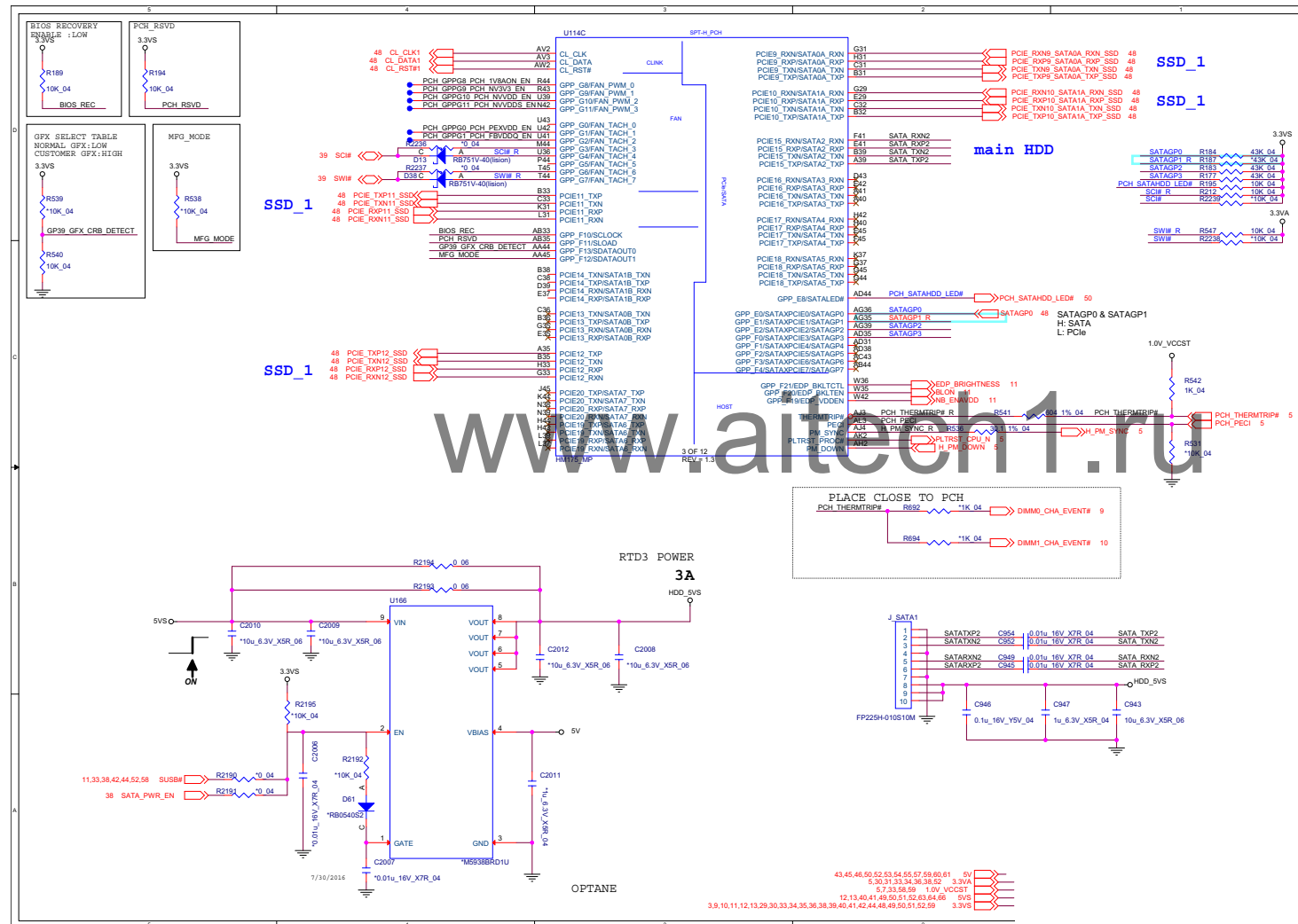


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## B.Schematic Diagrams

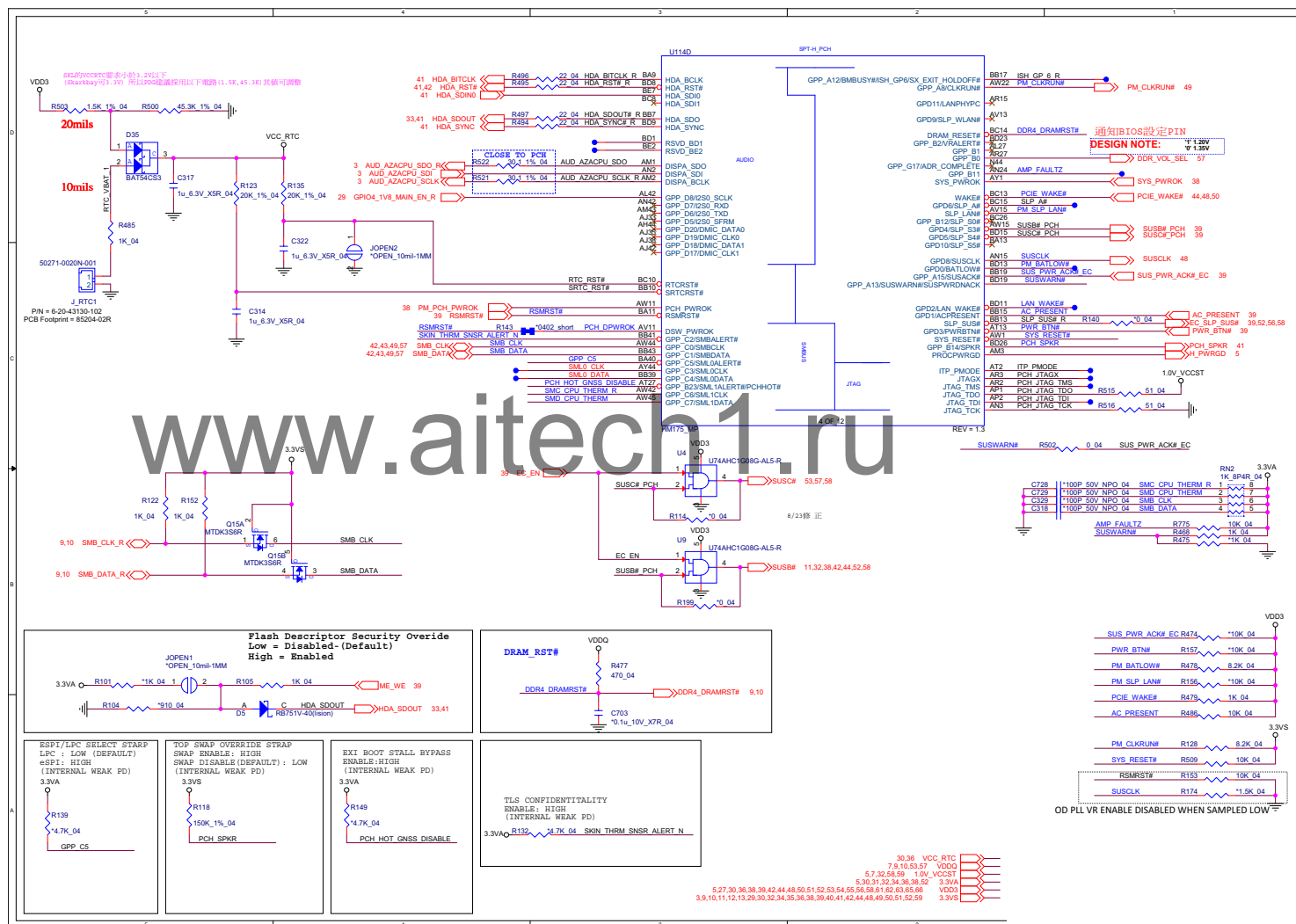
**Sheet 31 of 74**  
**PCH 2/9**



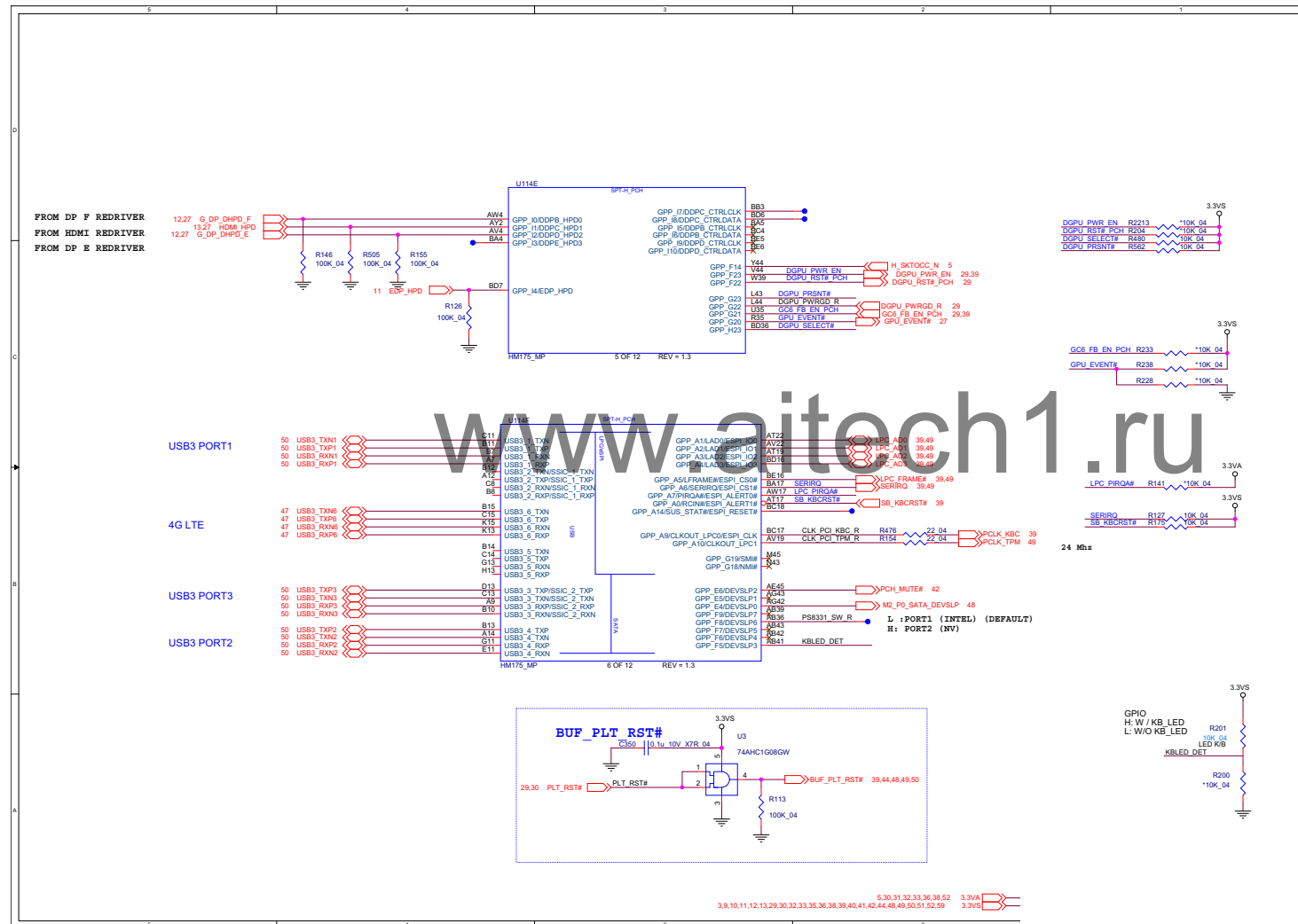


**PCH 4/9**

## B.Schematic Diagrams

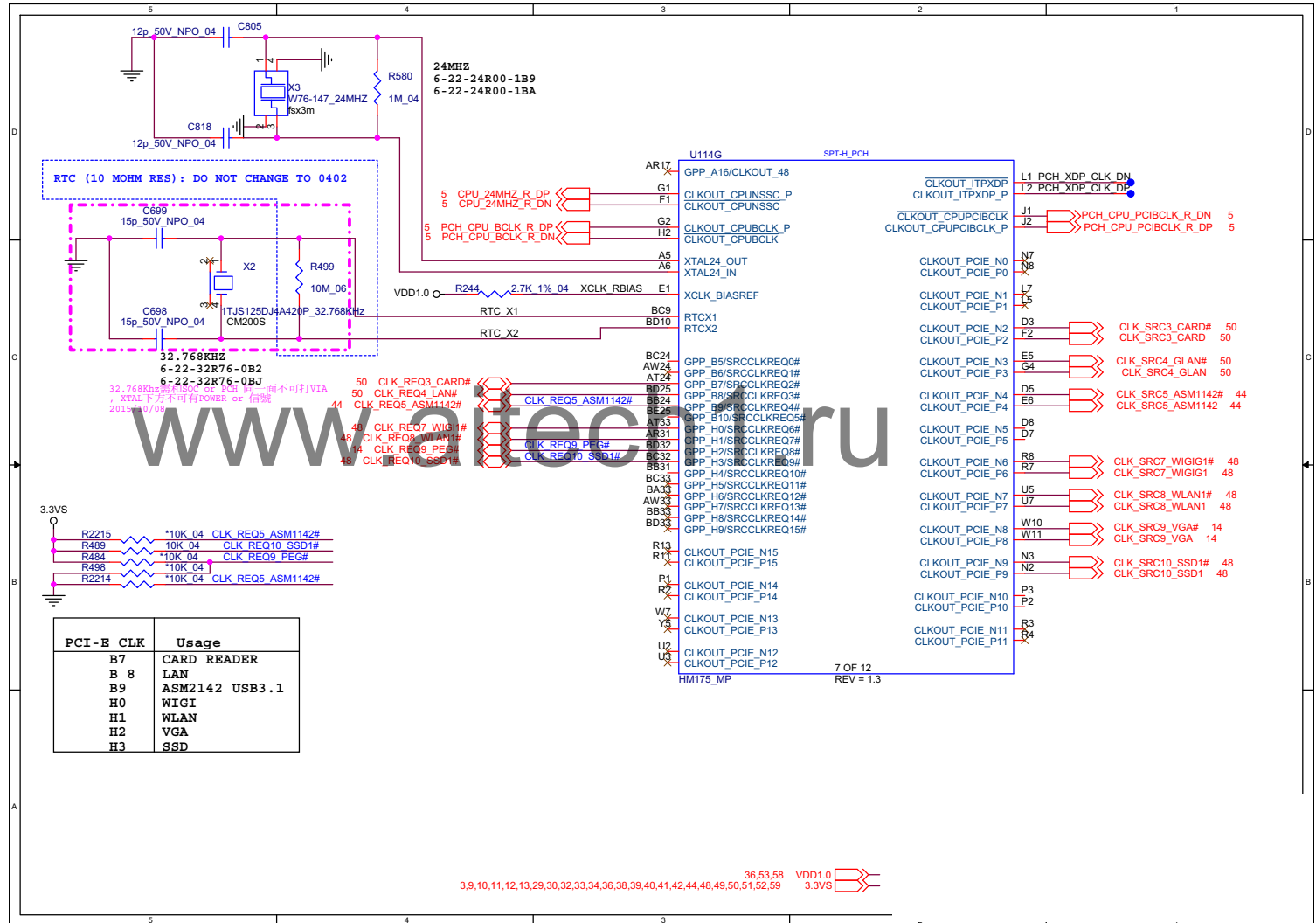


**PCH 5/9 B - 35**

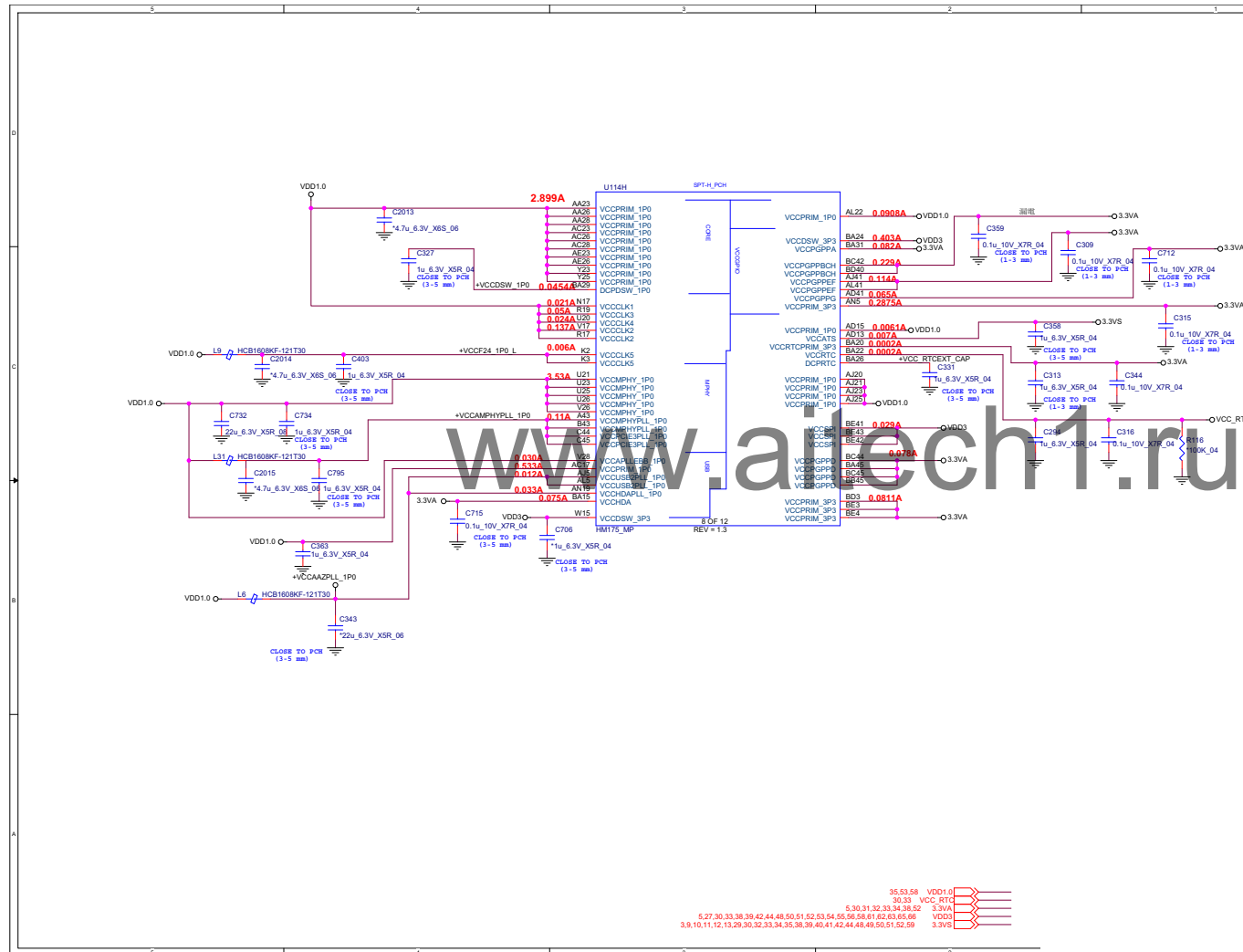


# PCH 6/9

Sheet 35 of 74  
PCH 6/9

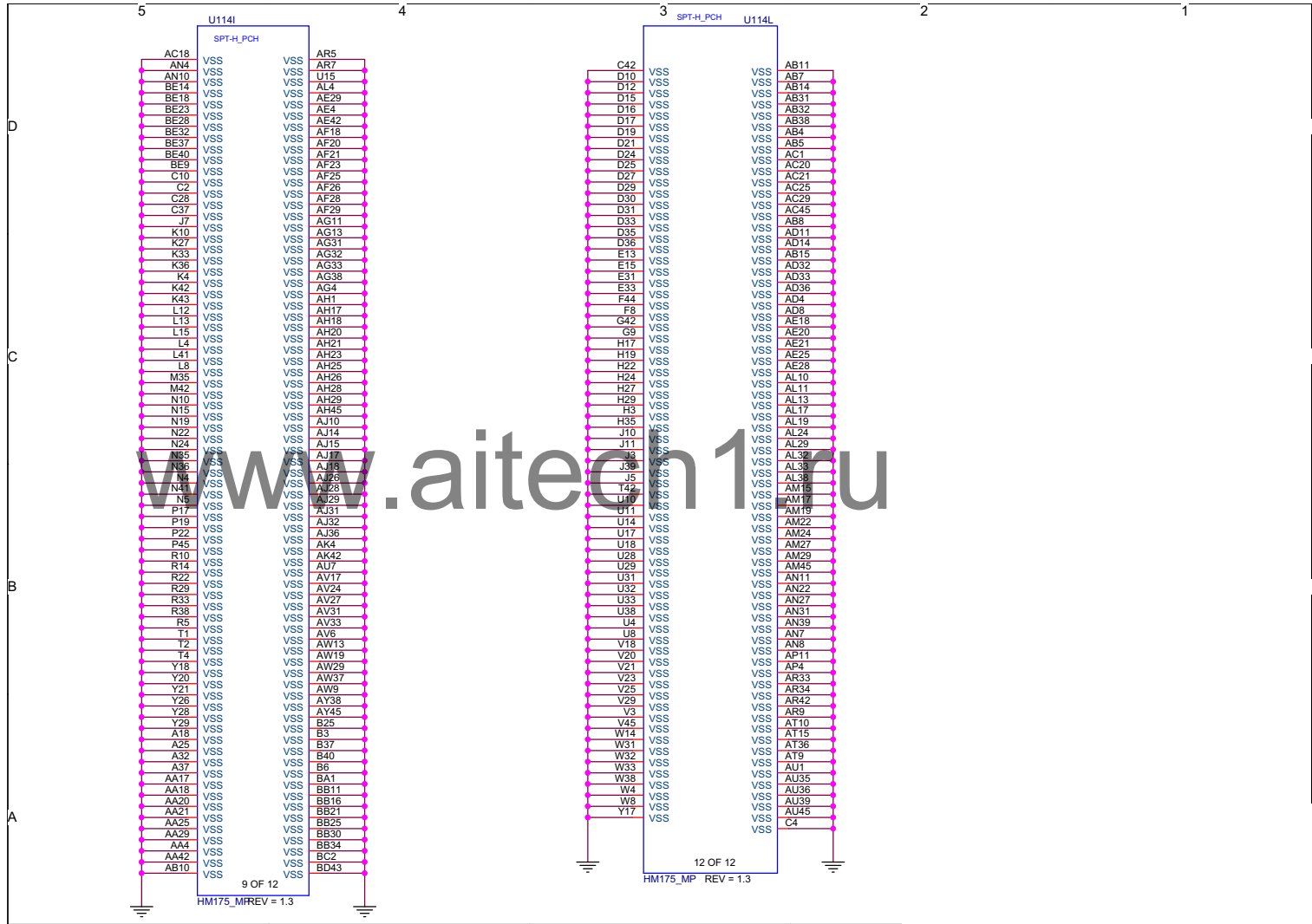


**PCH 7/9 B - 37**



PCH 8/9

Sheet 37 of 74  
PCH 8/9

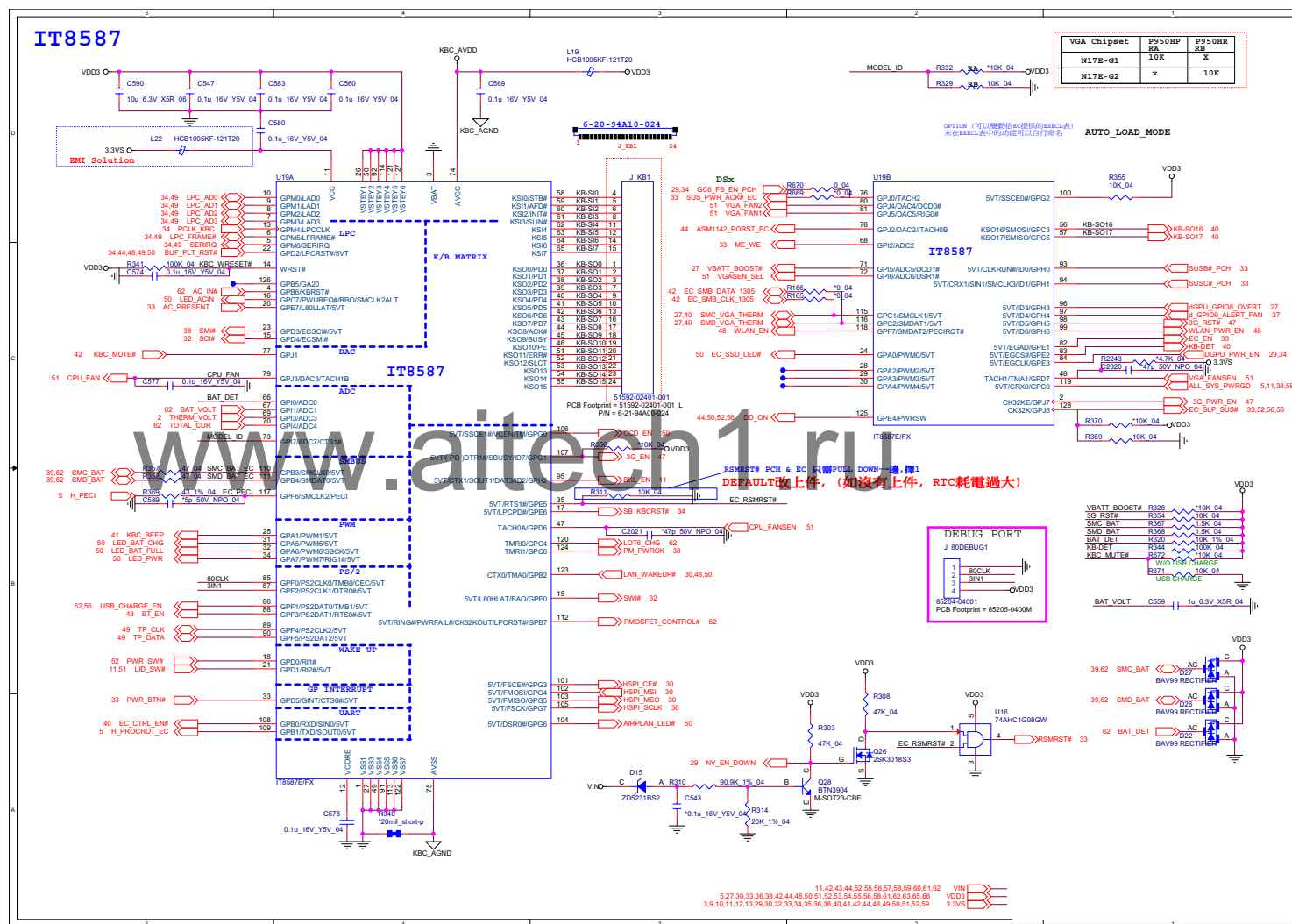


[illegible]

**KBC IT8587**

## B.Schematic Diagrams

Sheet 39 of 74  
KBC IT8587



BACKLIGHT KEYBOARD

不使用外部RESET, TLC59116F RESET# pin要pull high.

3.3VS

C704

R222 \*10K\_05

R232 \*10K\_05

R346 10K\_04

RGB K/B

27.39 SMC\_VGA\_THERM

27.39 SMD\_VGA\_THERM

39 EC\_CTRL\_EN#

R245

0.04

C423 1000p\_50V\_X7R\_04

TLC59116FIRHBR

RGB K/B

27 VCC

31 A0

32 A1

1 A2

2 A3

12 NC

13 NC2

28

24 RESET#

25 SCL

26 SDA

29

30 NC3

7 NC4

18 GND1

23 GND2

3 KBZONE1 B

4 KBZONE1 R

5 KBZONE1 G

6 KBZONE2 B

8 KBZONE2 R

9 KBZONE2 G

10 KBZONE3 B

11 KBZONE3 R

14 KBZONE3 G

15

16

17

19

20

21

22

OUT0

OUT1

OUT2

OUT3

OUT4

OUT5

OUT6

OUT7

OUT8

OUT9

OUT10

OUT11

OUT12

OUT13

OUT14

OUT15

KB-DET

KB-DET\_2

KB 5VS

R2205 \*28mil\_short-p

R2206 \*28mil\_short-p

RGB發光K/B用

FP226H-004S10M

KB-SO16

KB-SO17

KB-DET

KB-DET

J\_KBLED\_2

MAIN

RGB發光K/B用

KB\_5VS

C710 4.7u 6.3V\_X5R\_06

RGB K/B

5

12

11

10

9

8

7

6

5

4

3

2

1

KBZONE1 R

KBZONE1 G

KBZONE1 B

KBZONE2 R

KBZONE2 G

KBZONE2 B

KBZONE3 R

KBZONE3 G

KBZONE3 B

NC1

NC2

J\_KBLED\_1

FP226H-012S10M

6-20-94K50-012

RGB K/B

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3,9,10,11,12,13,29,30,32,33,34,35,36,38,39,41,42,44,48,49,50,51,52,59

5,27,30,33,36,38,39,42,44,48,50,51,52,53,54,55,56,58,61,62,63,65,66

5VS

3.3VS

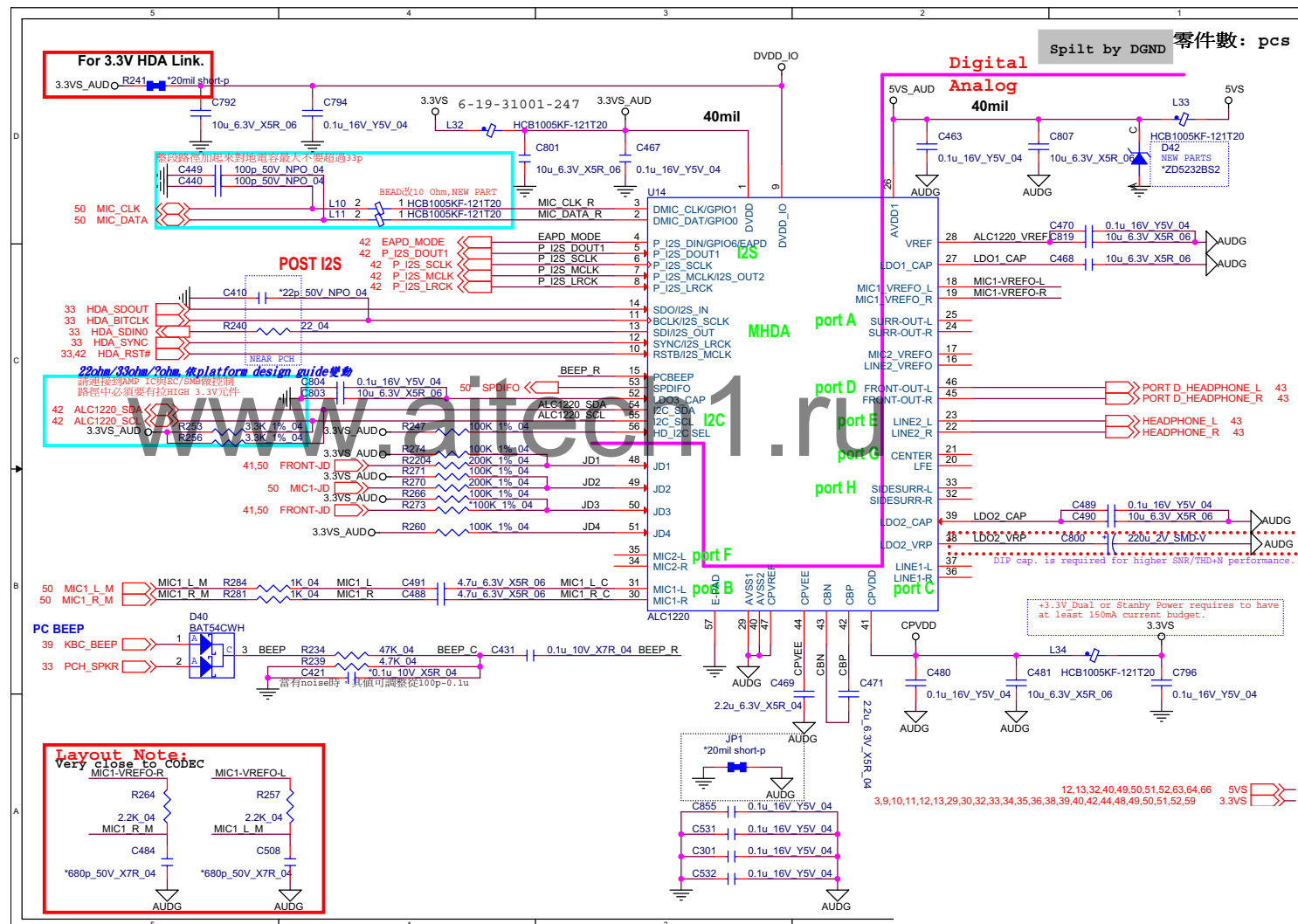
VDD3

## B.Schematic Diagrams

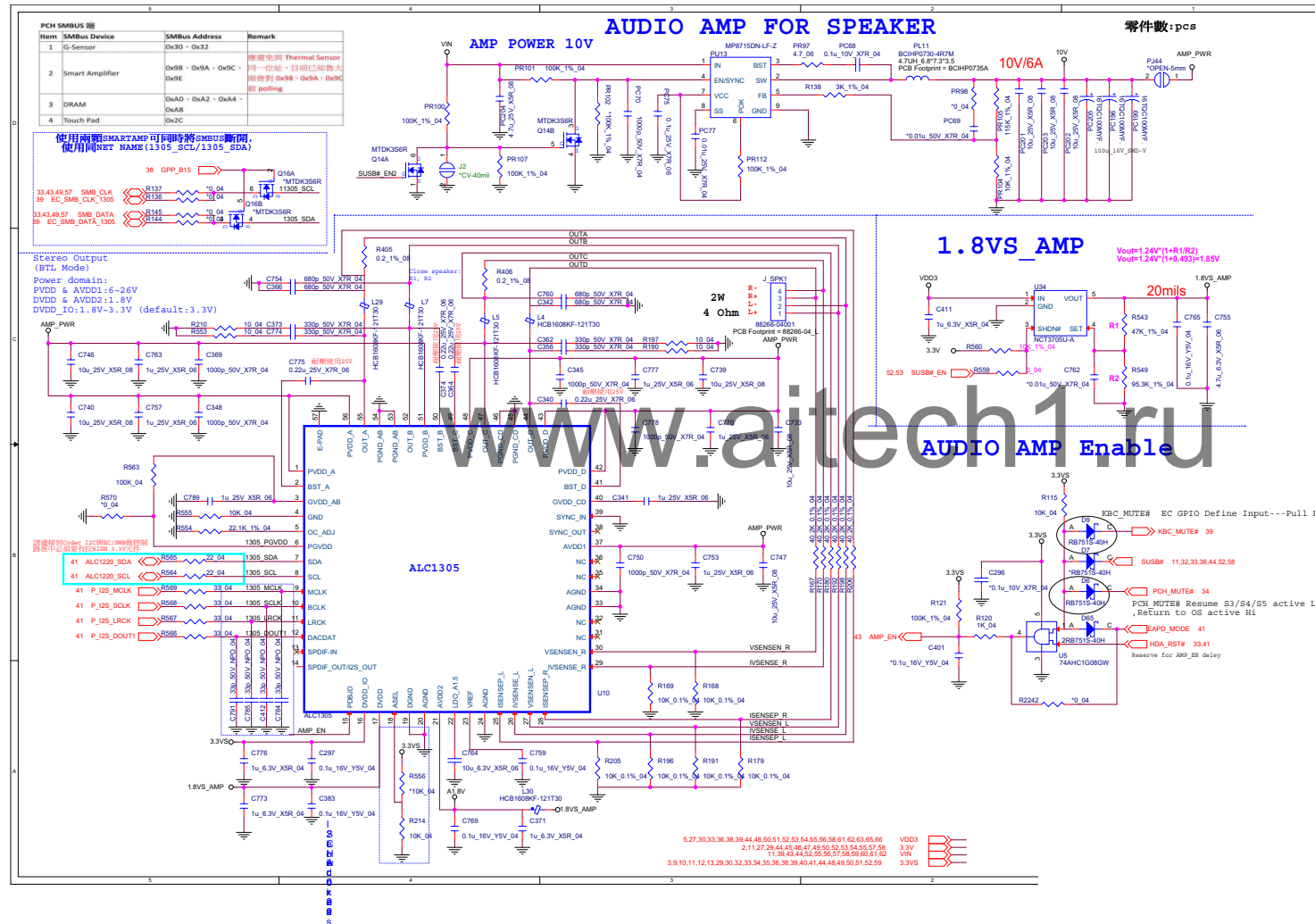
# Realtek ALC1220

## B. Schematic Diagrams

Sheet 41 of 74  
Realtek ALC1220



## Smart AMP ALC1305



## 3D HeadPhone AMP

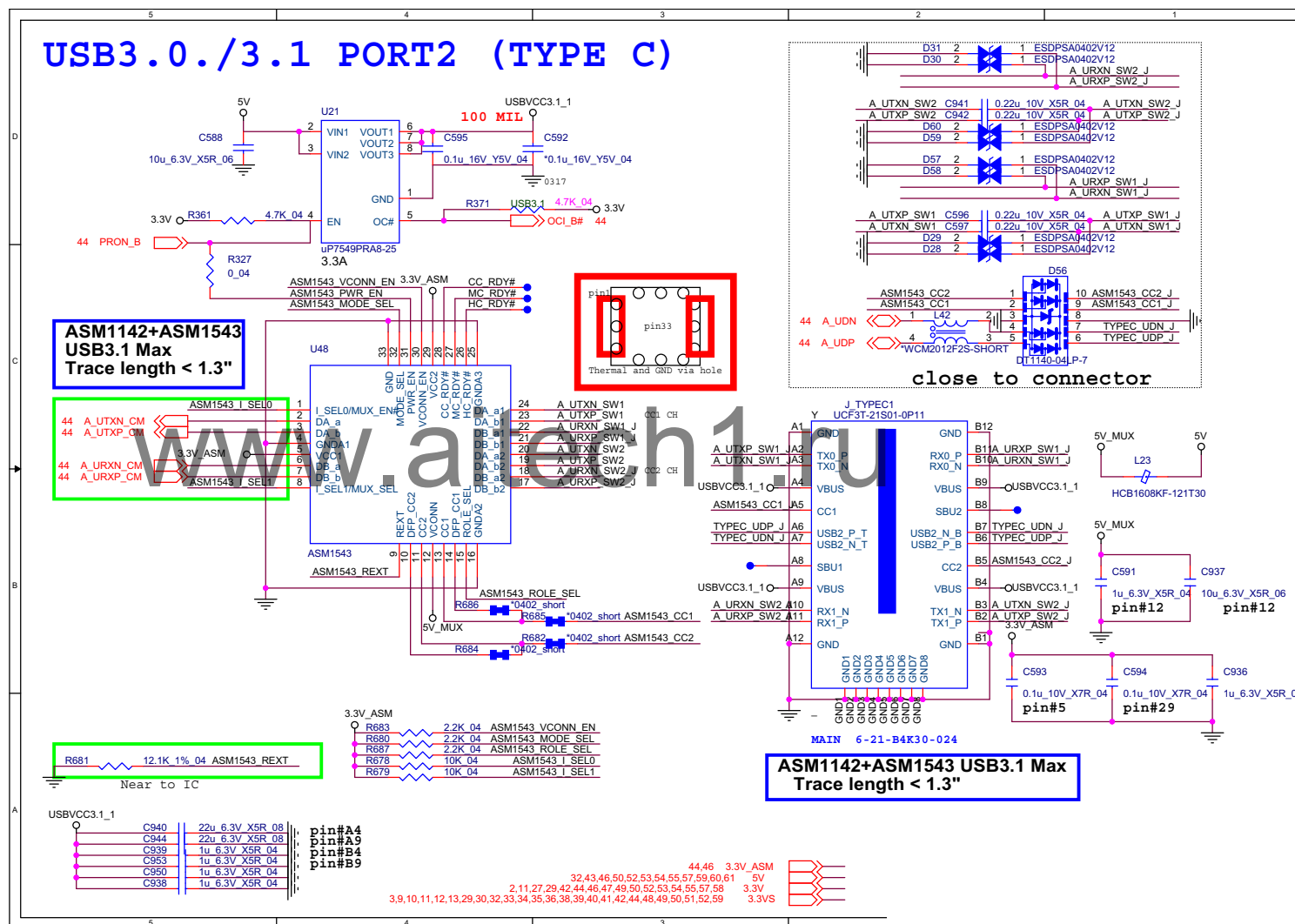


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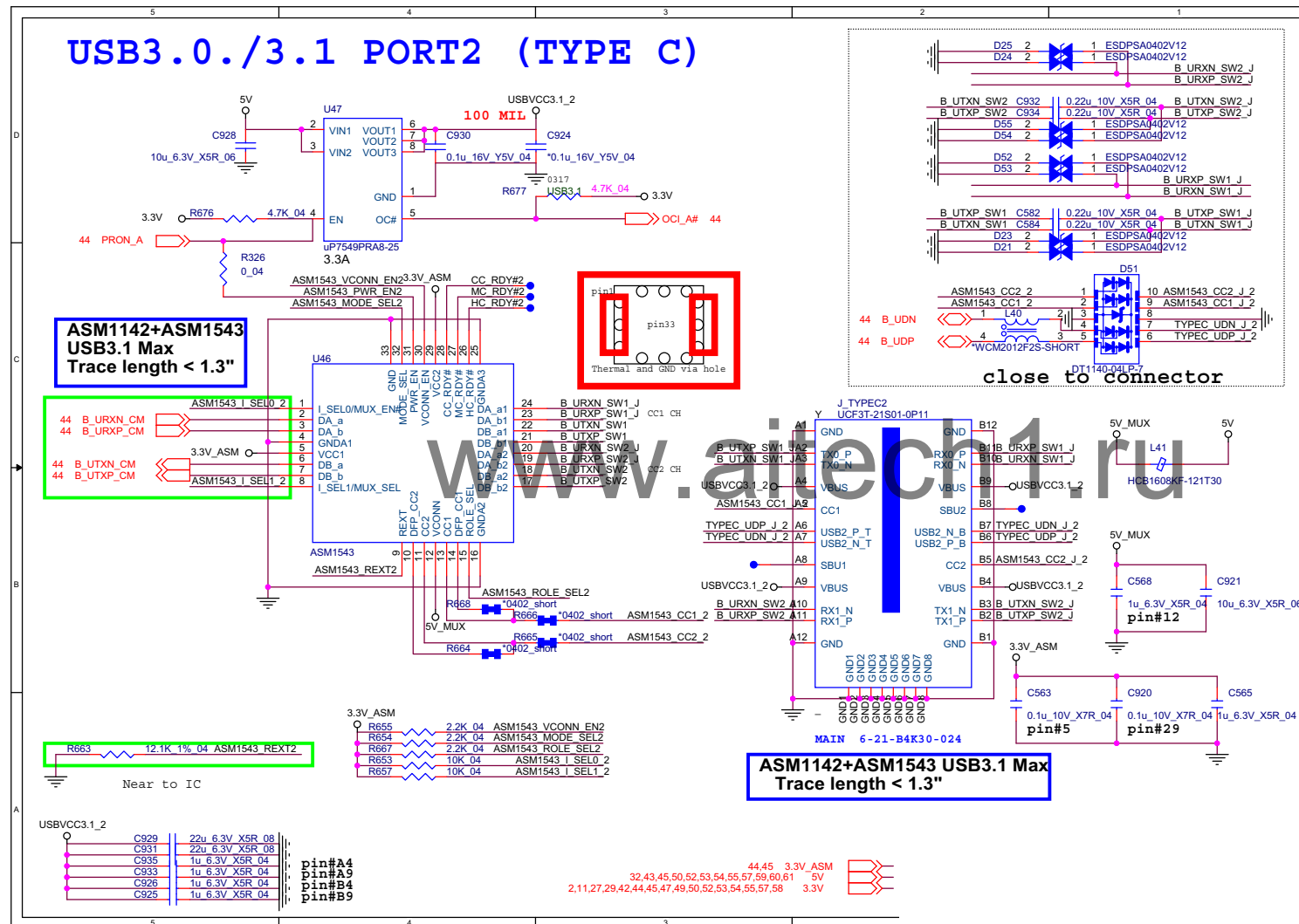
# ASM2142 2/3

## B. Schematic Diagrams

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ASM2142 2/3



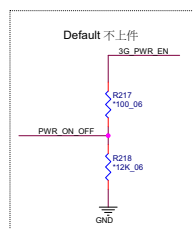
## ASM2142 3/3

Sheet 46 of 74  
ASM2142 3/3

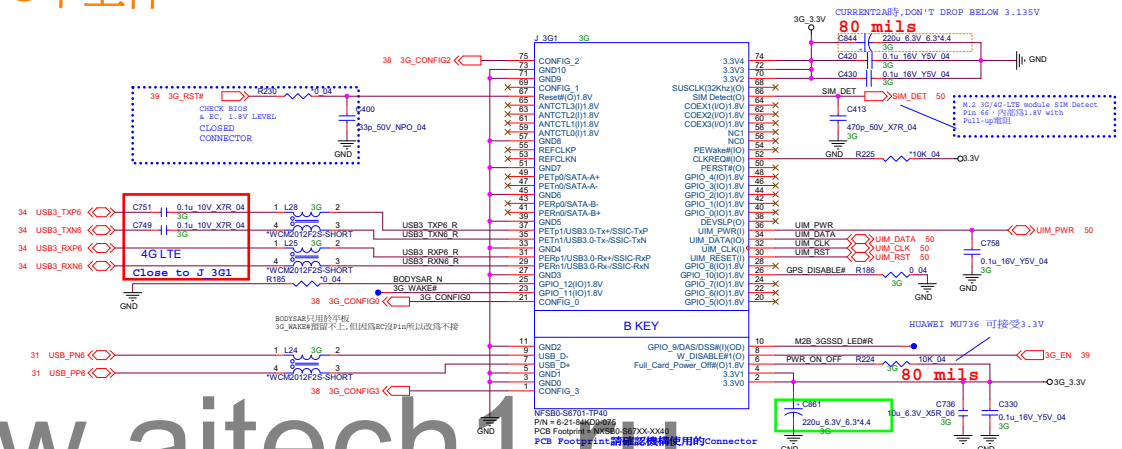
## M.2 3G/LTE

Only P670RS 3G不上件

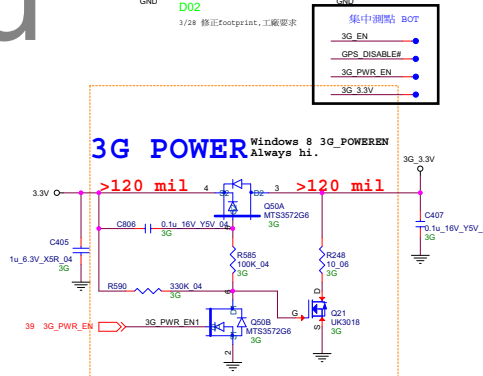
3G /LTE CARD USB3.0



Sheet 47 of 74  
M.2 3G/LTE



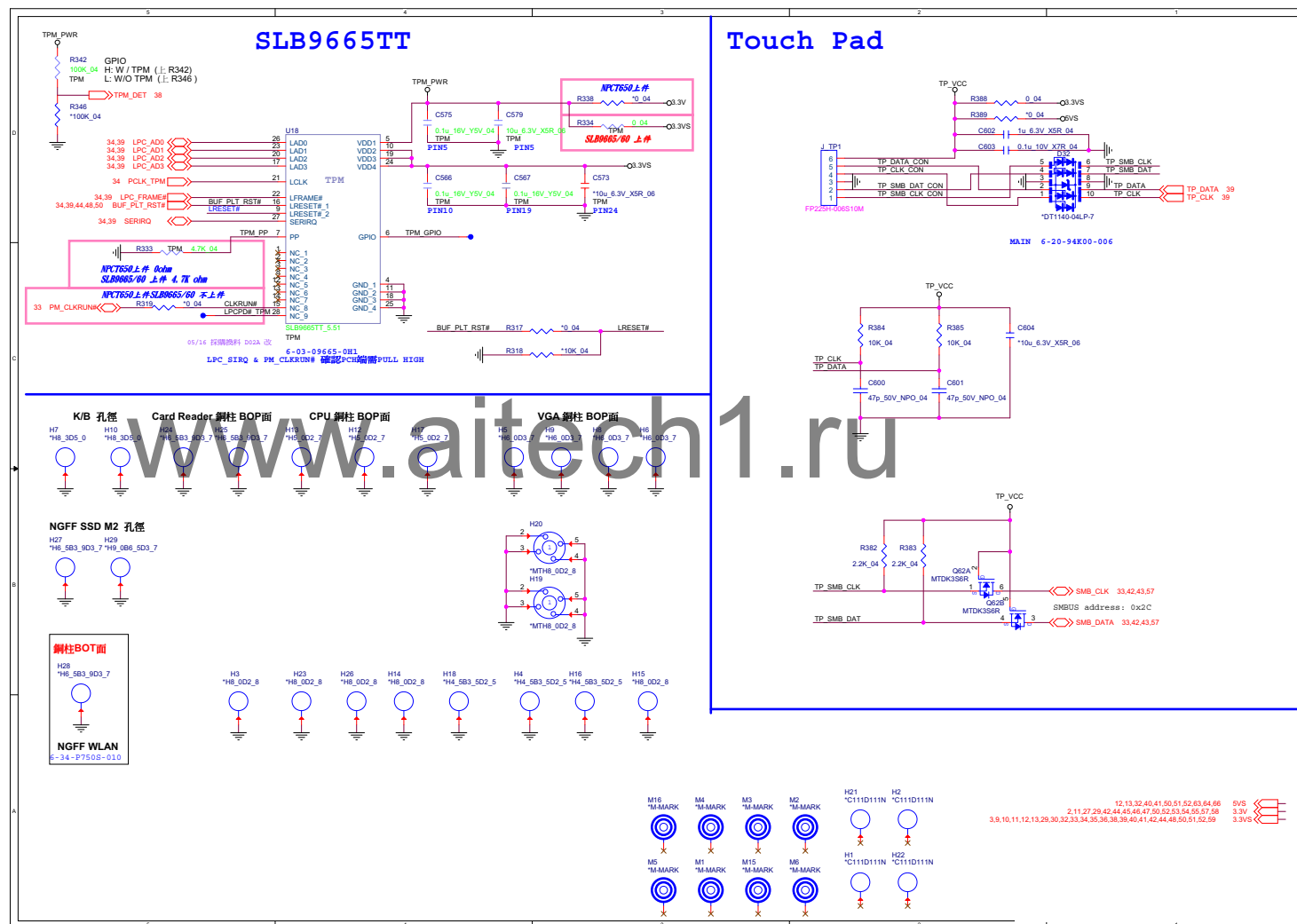
www.aitech1.ru



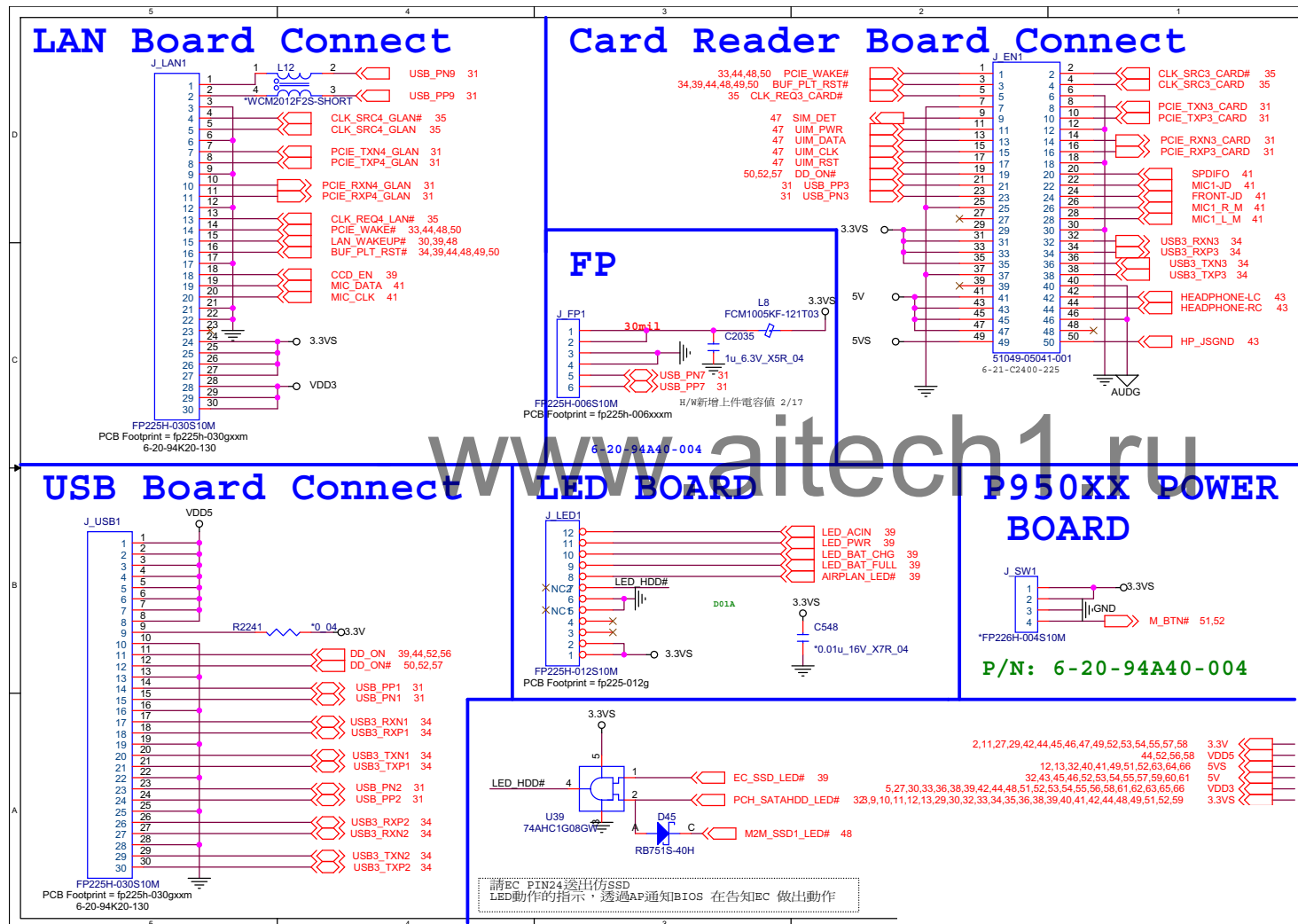
2.11.27.29.42.44.45.46.49.50.52.53.54.55.57.58 3.3V 



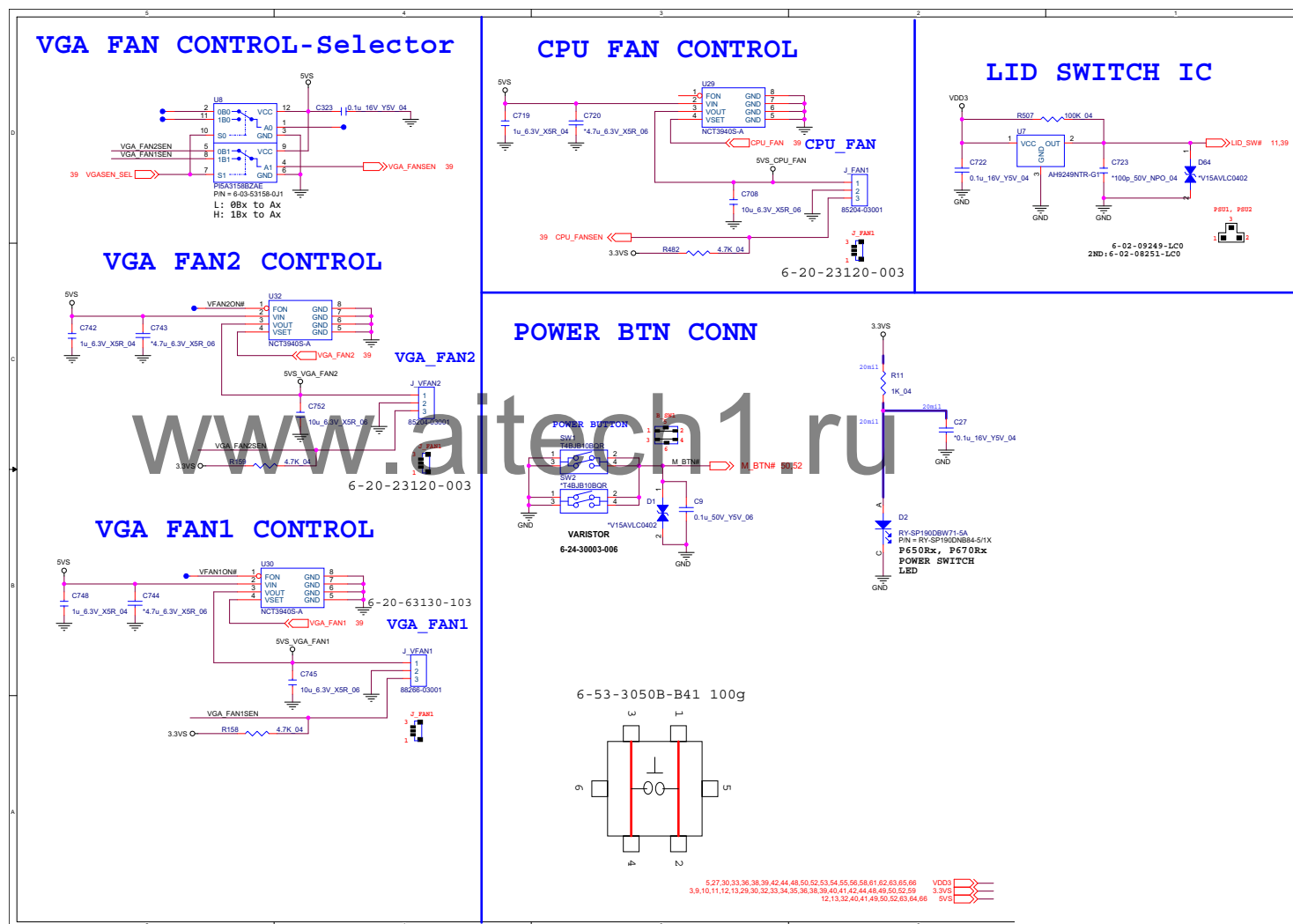
Sheet 49 of 74  
TPM, TP



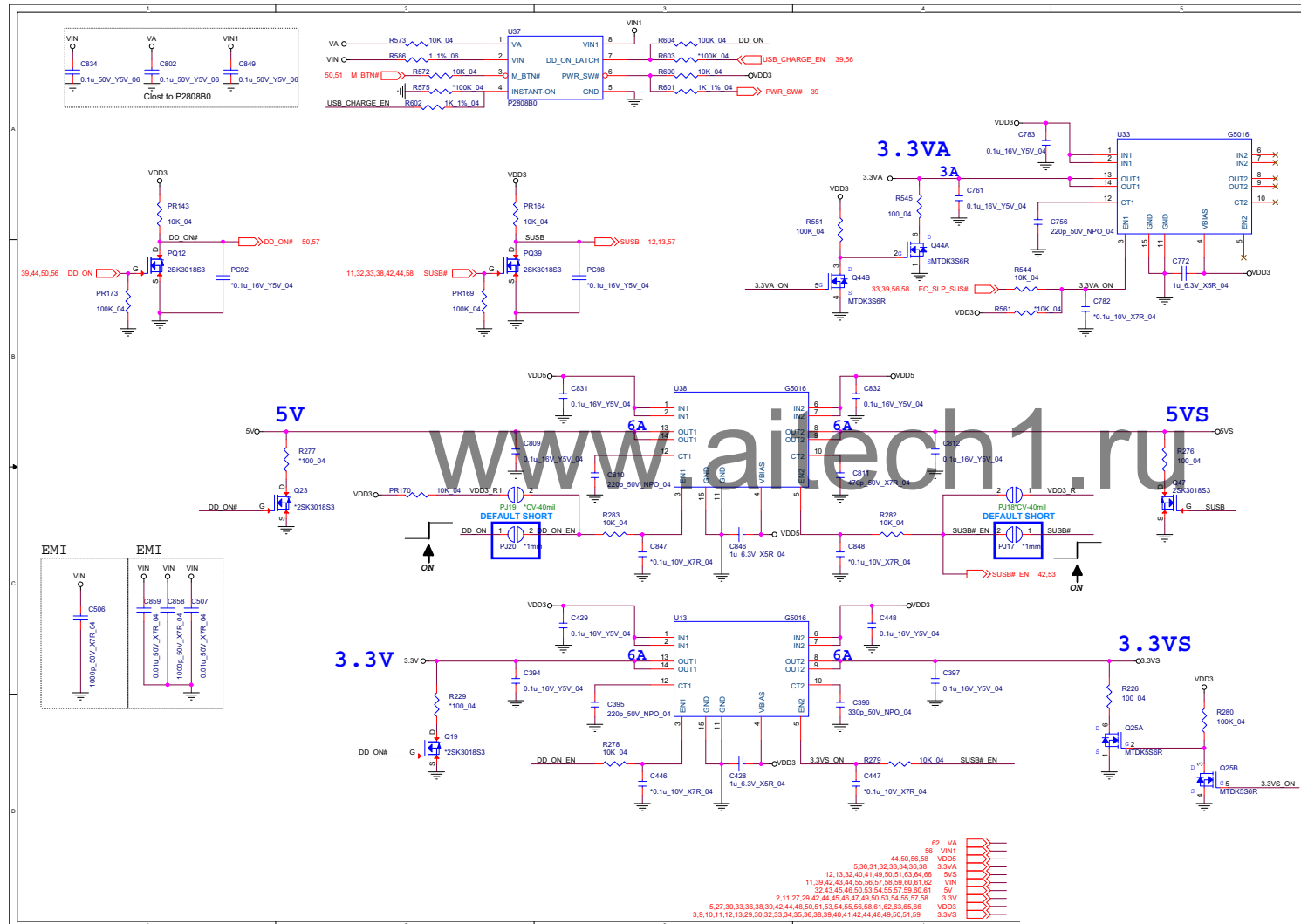
## Connector

Sheet 50 of 74  
Connector

Sheet 51 of 74  
Fan, LID, KB LED



# 5V, 5VS, 3.3V, 3.3VS, 3.3VA

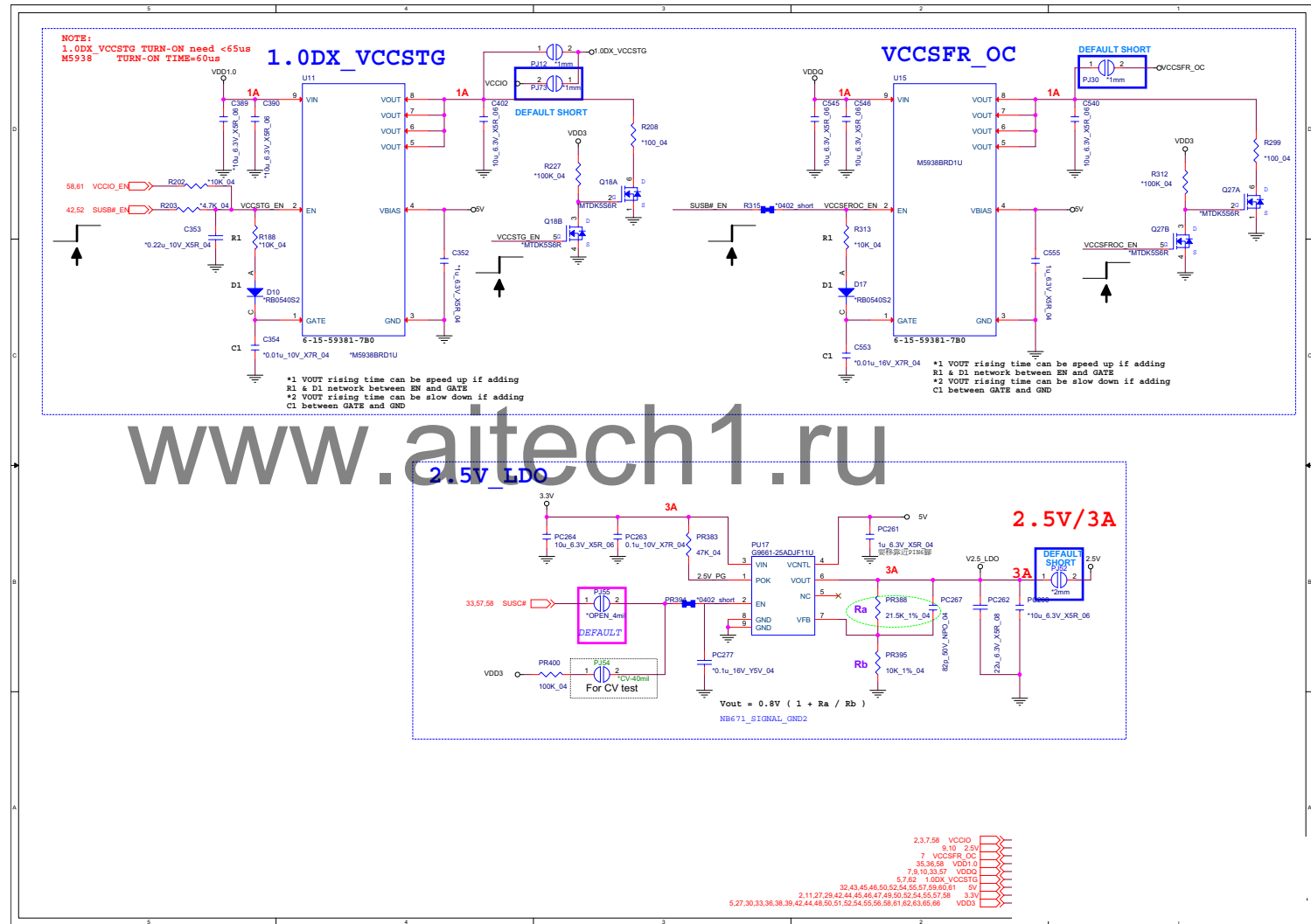


Sheet 52 of 74  
5V, 5VS, 3.3V,  
3.3VS, 3.3VA

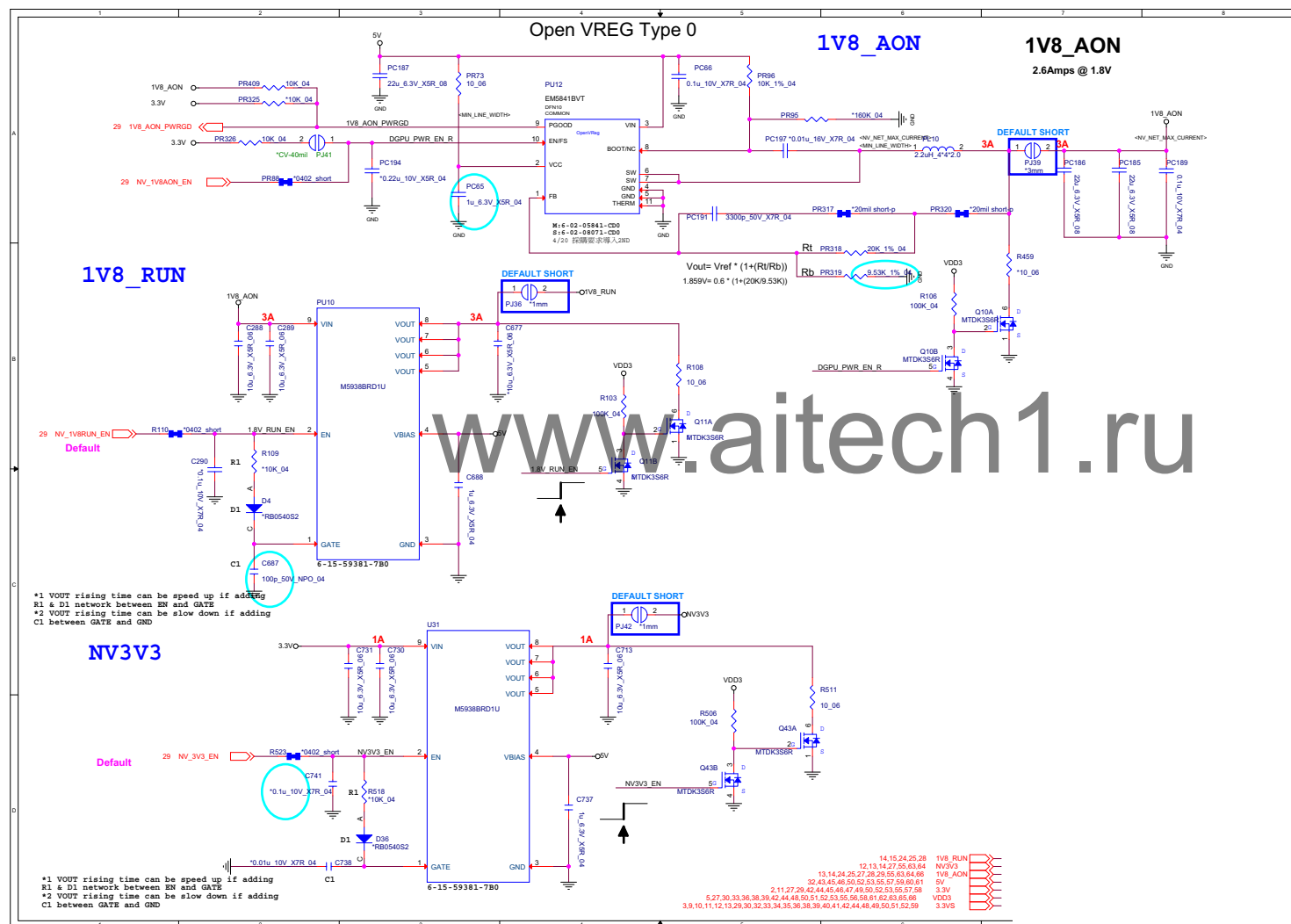
## Schematic Diagrams

## 1.0DX\_VCCSTG/VCCSFR\_OC/2.5V

Sheet 53 of 74  
1.0DX\_VCCSTG/  
VCCSFR\_OC/2.5V



## 1V8\_RUN/AON, NV3V3

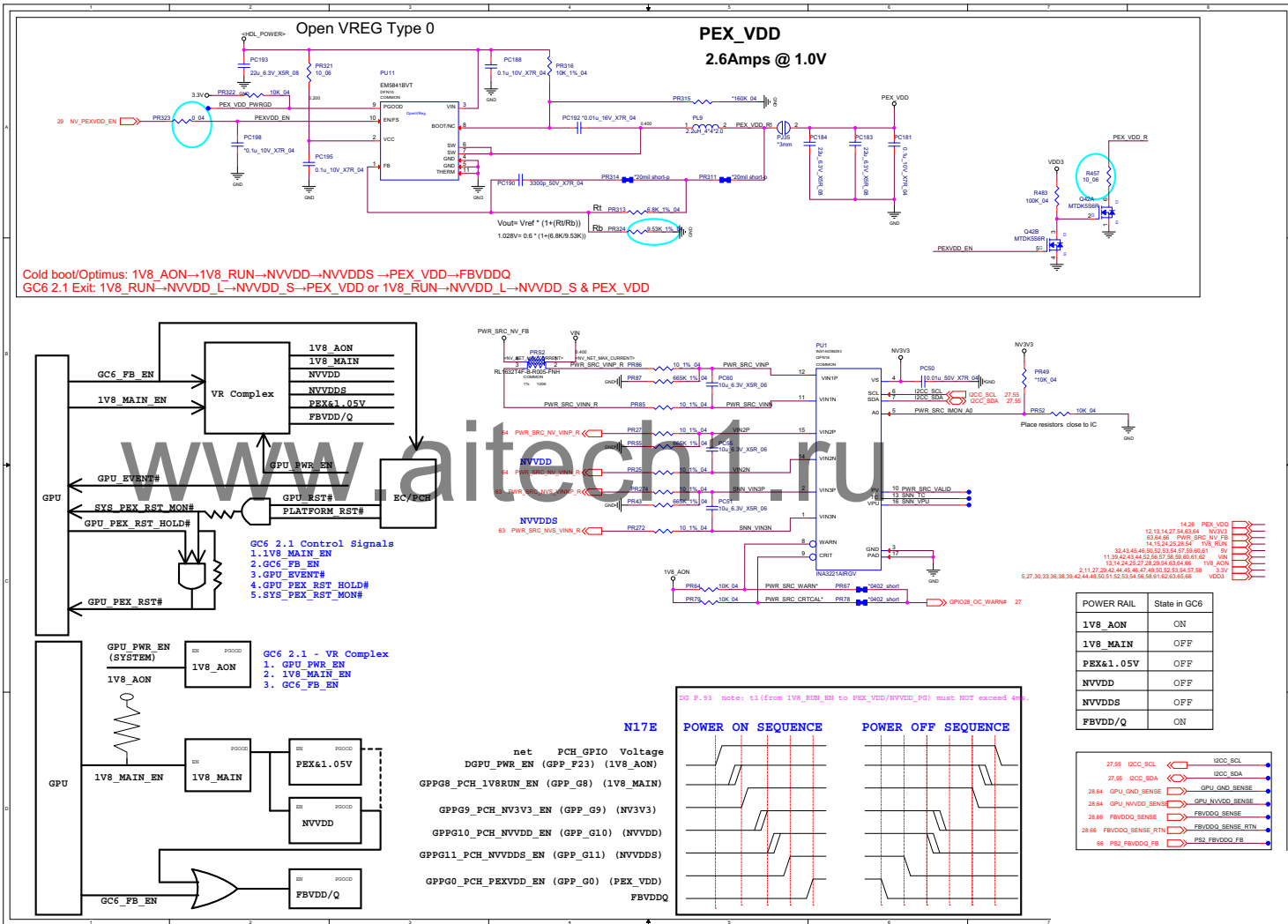


Sheet 54 of 74  
1V8\_RUN/AON,  
NV3V3

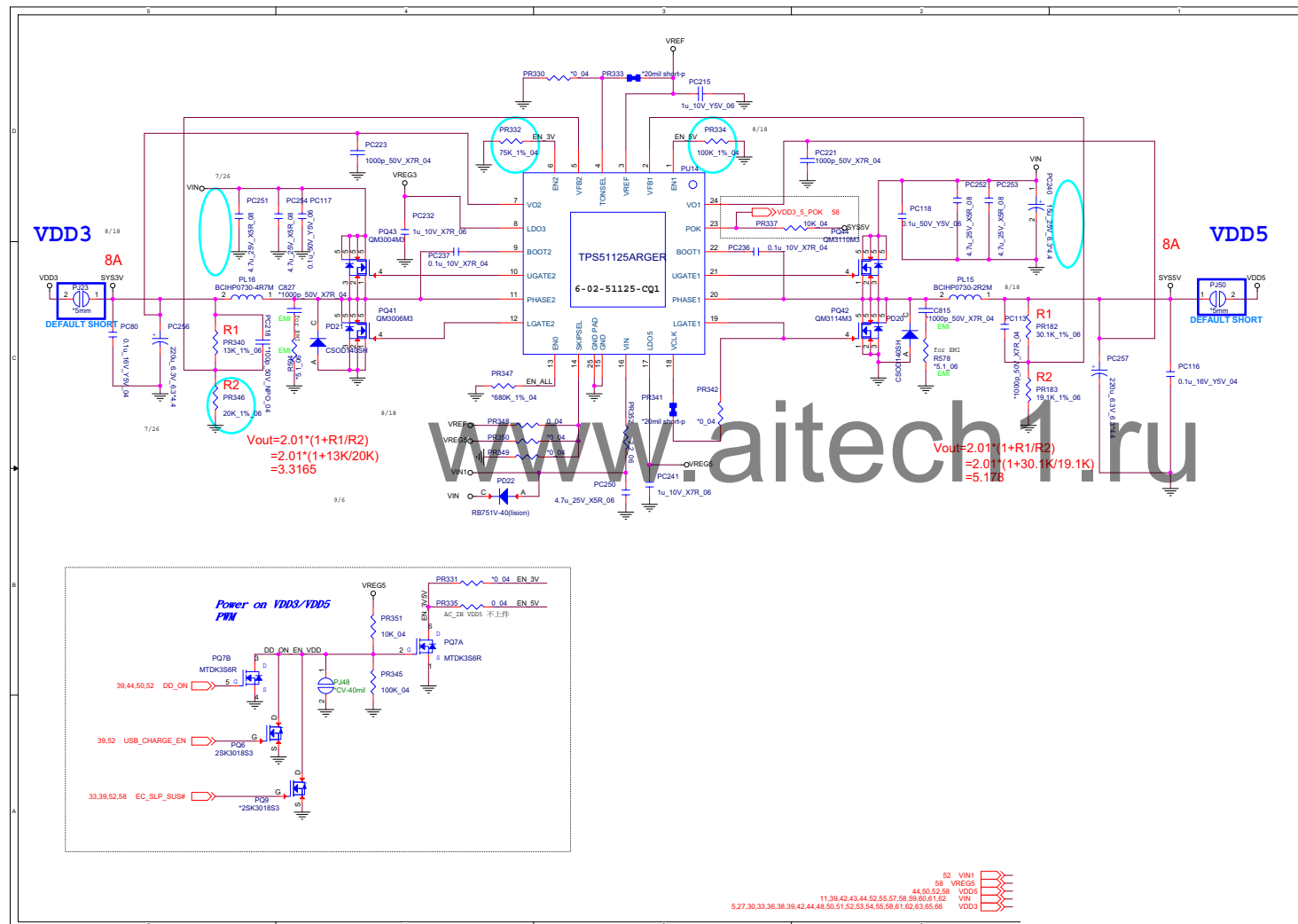
Schematic Diagrams

PEX\_VDD

Sheet 55 of 74  
PEX\_VDD

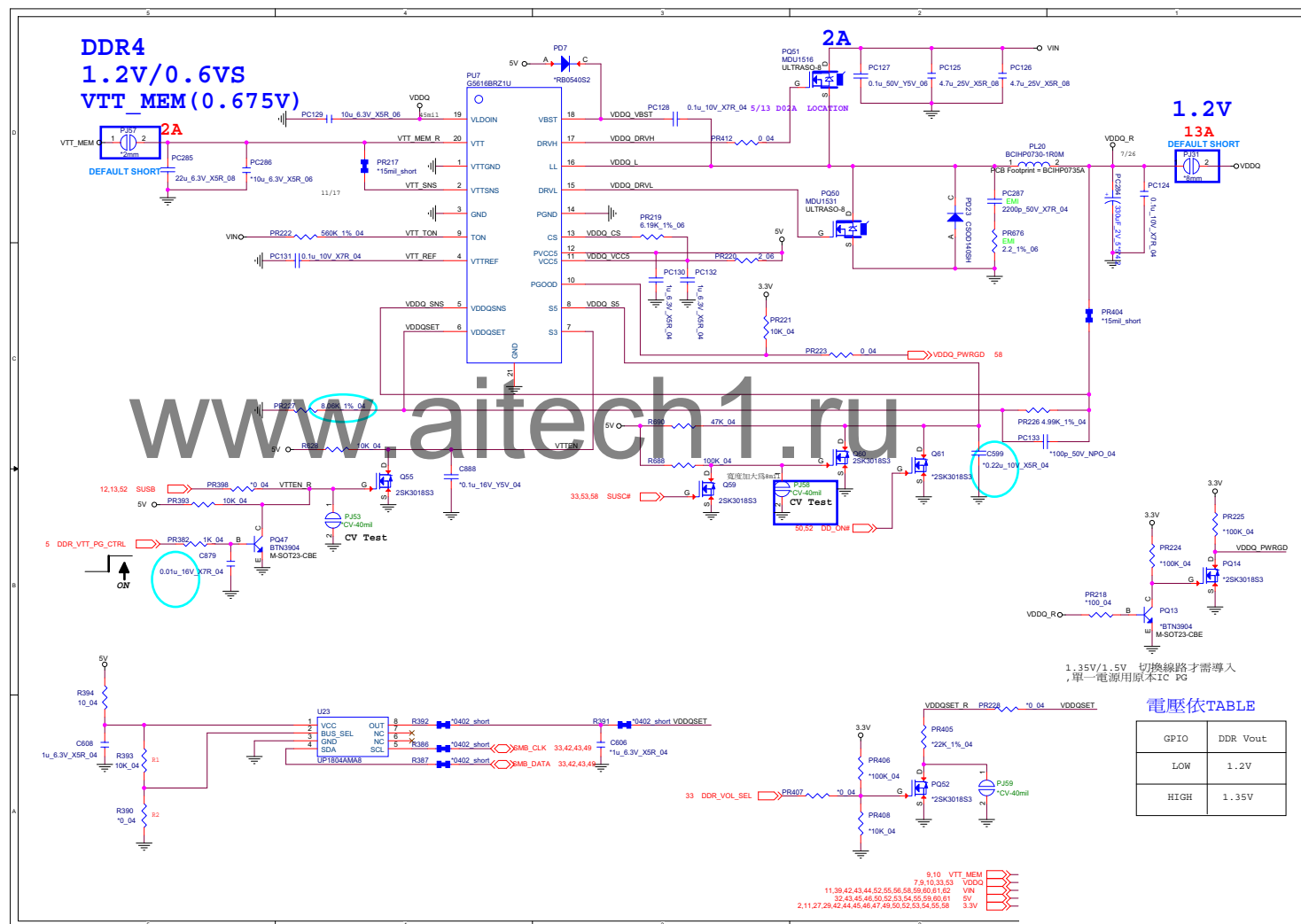


## VDD3, VDD5 B - 57

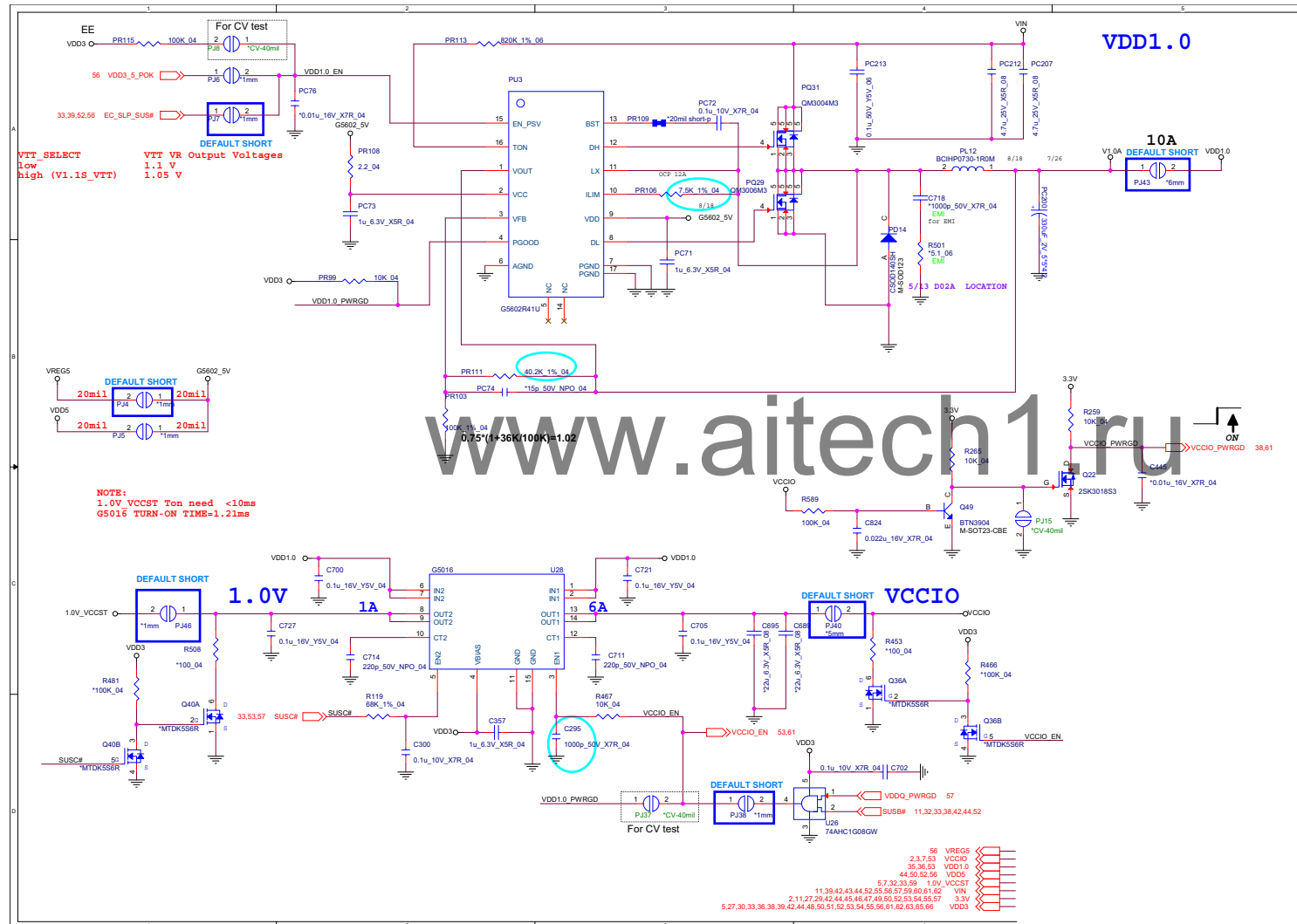


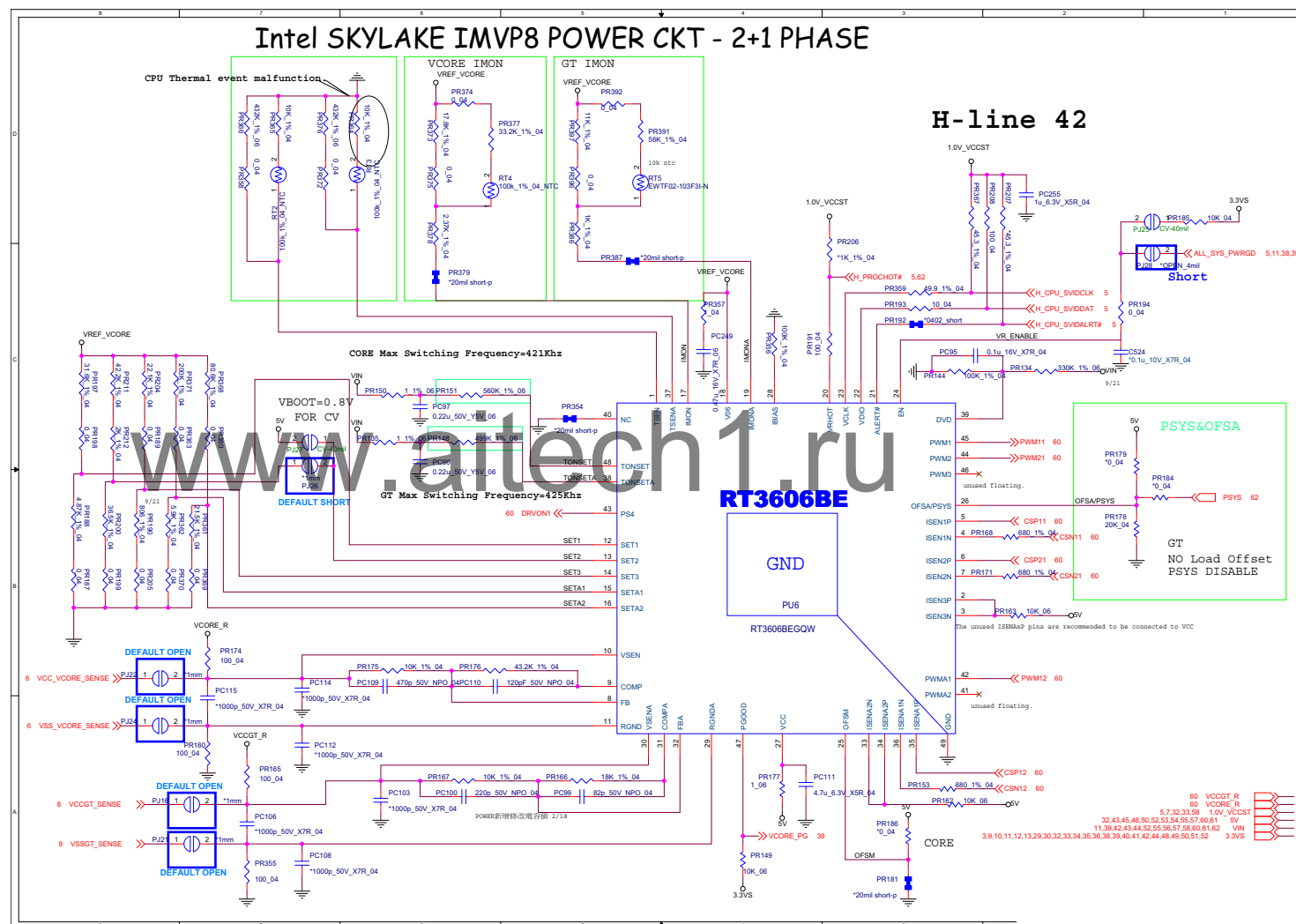
## DDR 1.2V / 0.6VS

Sheet 57 of 74  
DDR 1.2V / 0.6VS



ver 1.0V, VCCIO B - 59



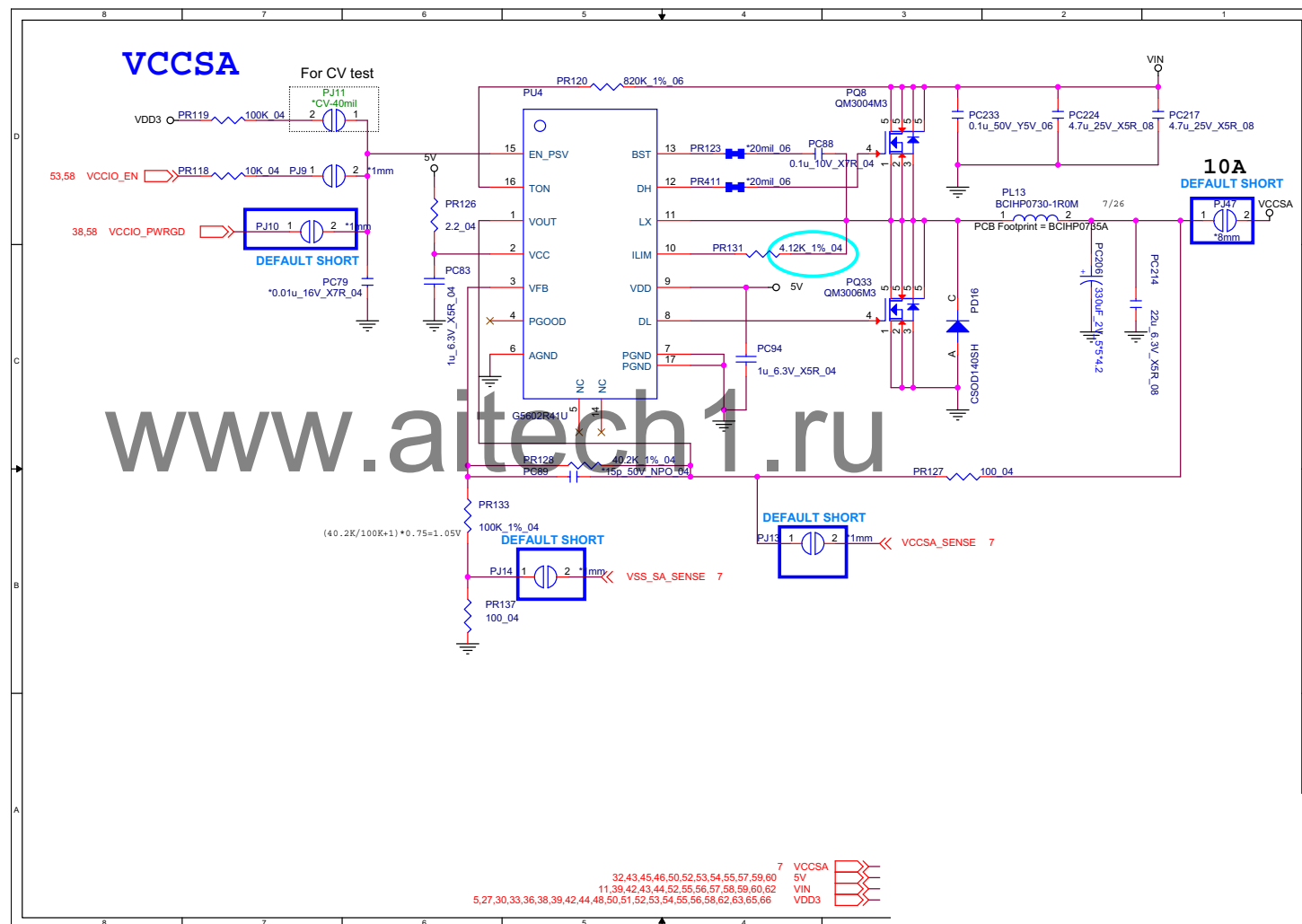


The image shows a detailed PCB layout for the Vcore and VCCGT output stage. The layout is organized into three main sections: 2A, 4A, and 10A. Each section represents a different power output stage.

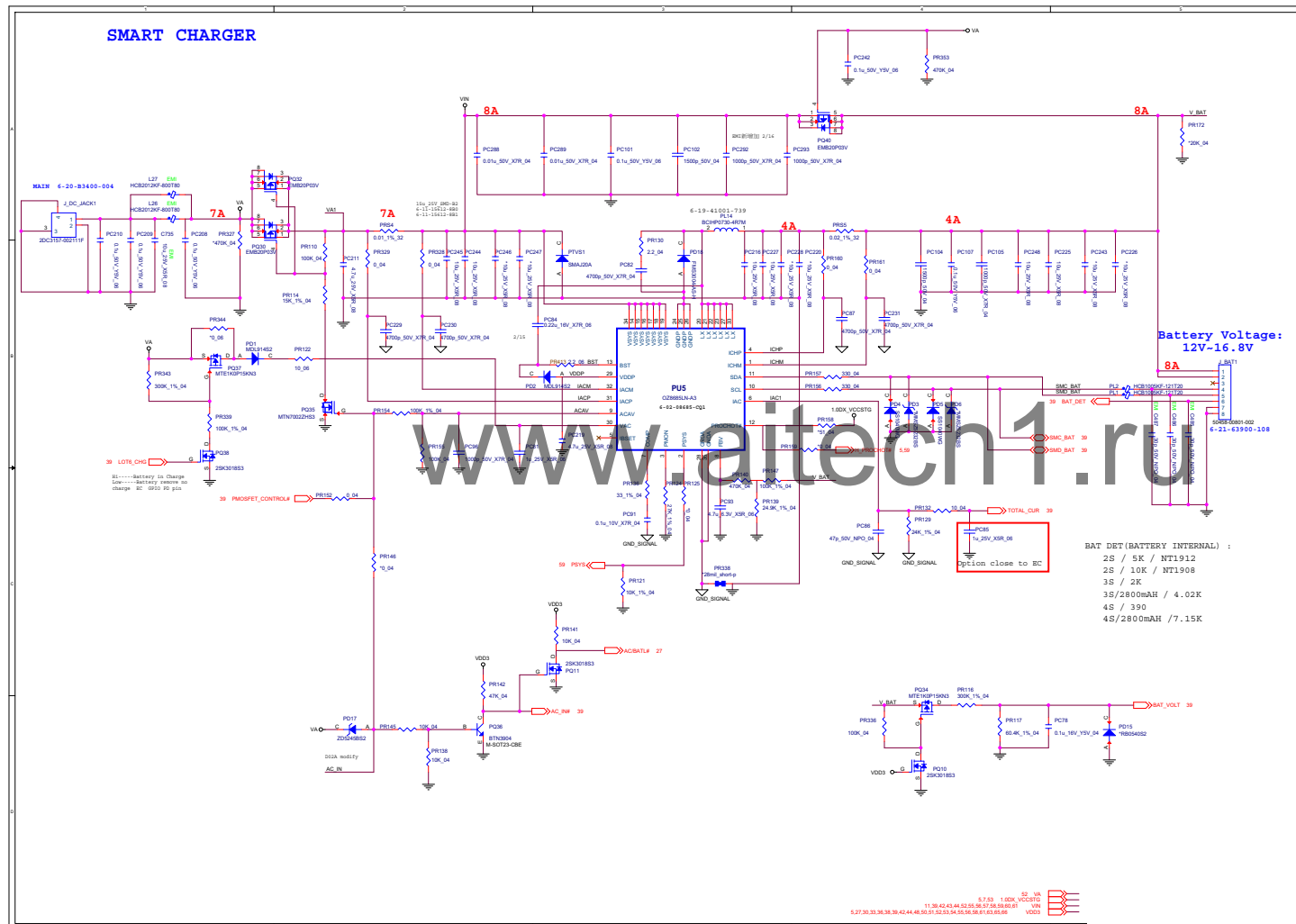
- 2A Section:** This section is located at the bottom of the layout. It features a PMIC (PQ54) and its associated components, including capacitors (e.g., 100nF, 10uF, 100uF) and inductors (e.g., 100nH, 10uH, 100uH). The output is labeled VCCGT\_R.
- 4A Section:** This section is located at the top of the layout. It features a PMIC (PQ54) and its associated components, including capacitors (e.g., 100nF, 10uF, 100uF) and inductors (e.g., 100nH, 10uH, 100uH). The output is labeled Vcore\_R.
- 10A Section:** This section is located on the right side of the layout. It features a PMIC (PQ54) and its associated components, including capacitors (e.g., 100nF, 10uF, 100uF) and inductors (e.g., 100nH, 10uH, 100uH). The output is labeled Vcore\_R.

The layout includes various components like capacitors (e.g., 100nF, 10uF, 100uF), inductors (e.g., 100nH, 10uH, 100uH), and connectors (e.g., 100pin, 100pin). The layout also includes a large watermark 'www.aitech1.ru' across the center.

The diagram shows a 4-to-1 multiplexer implemented using two 2-to-1 multiplexers. The top 2-to-1 multiplexer has inputs  $a$  and  $b$ , and its output is  $c$ . The bottom 2-to-1 multiplexer has inputs  $d$  and  $c$ , and its output is  $e$ . The select lines for both multiplexers are  $s_1$  and  $s_0$ .

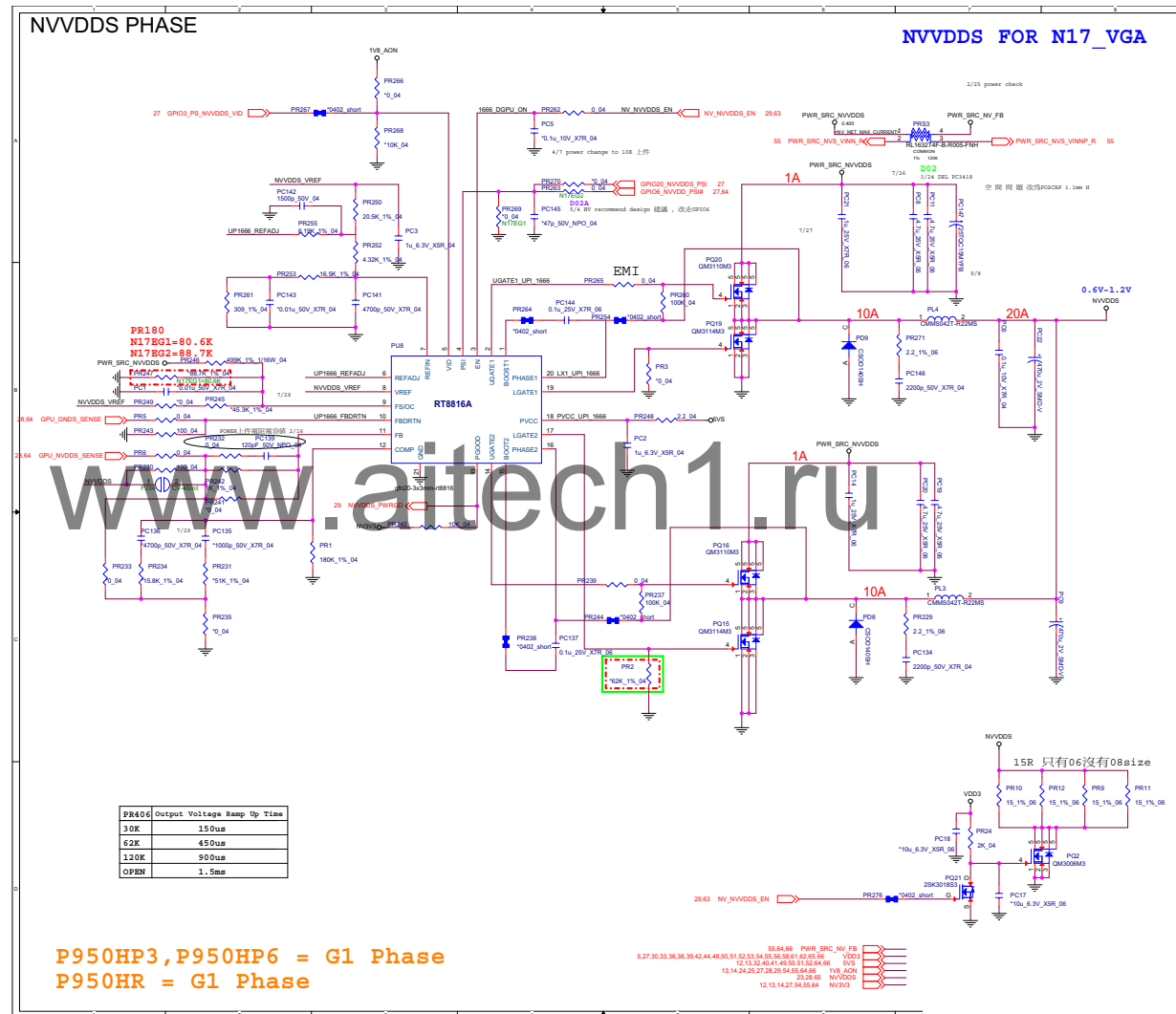


**AC\_In, Charger B - 63**

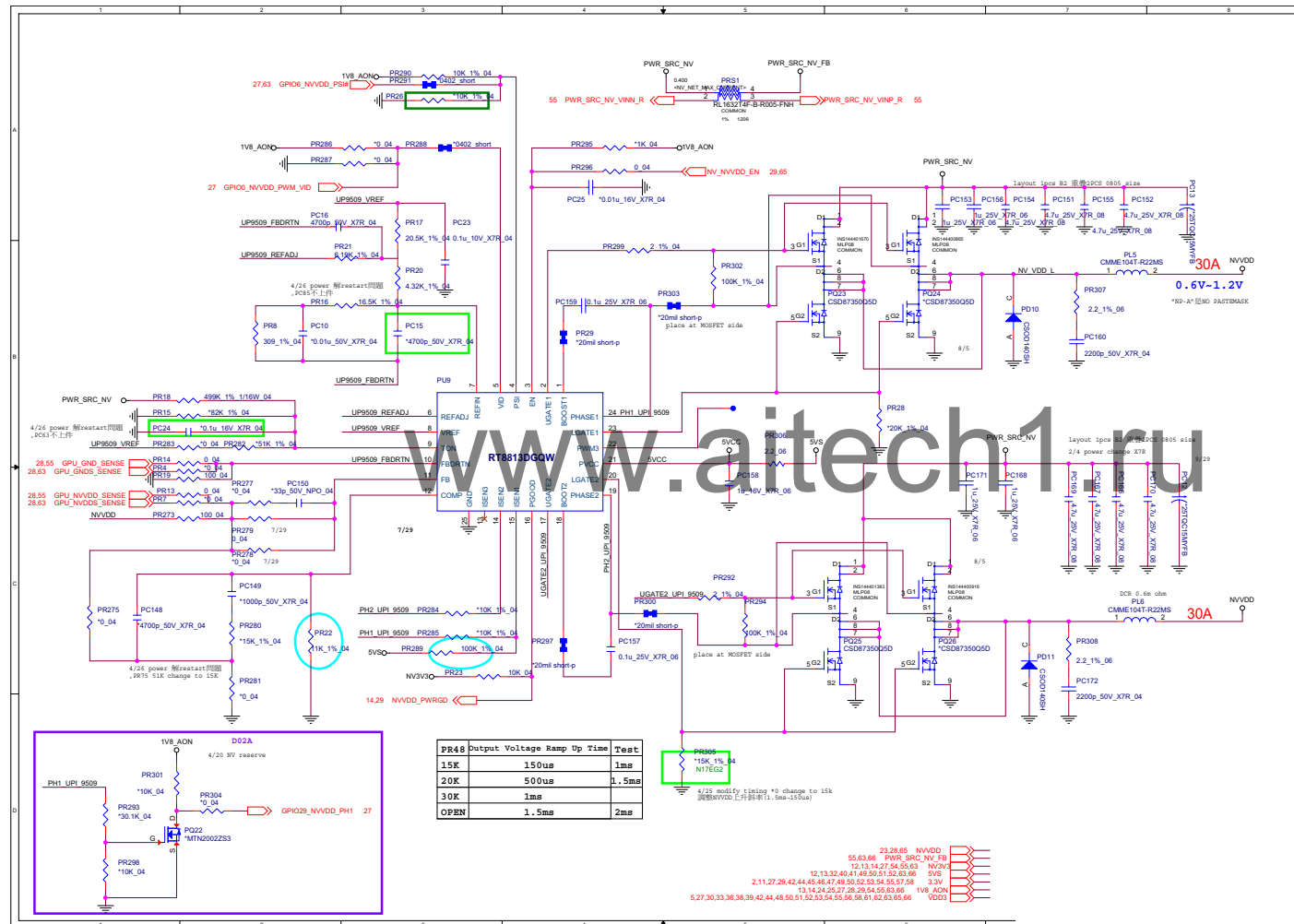


## Schematic Diagrams

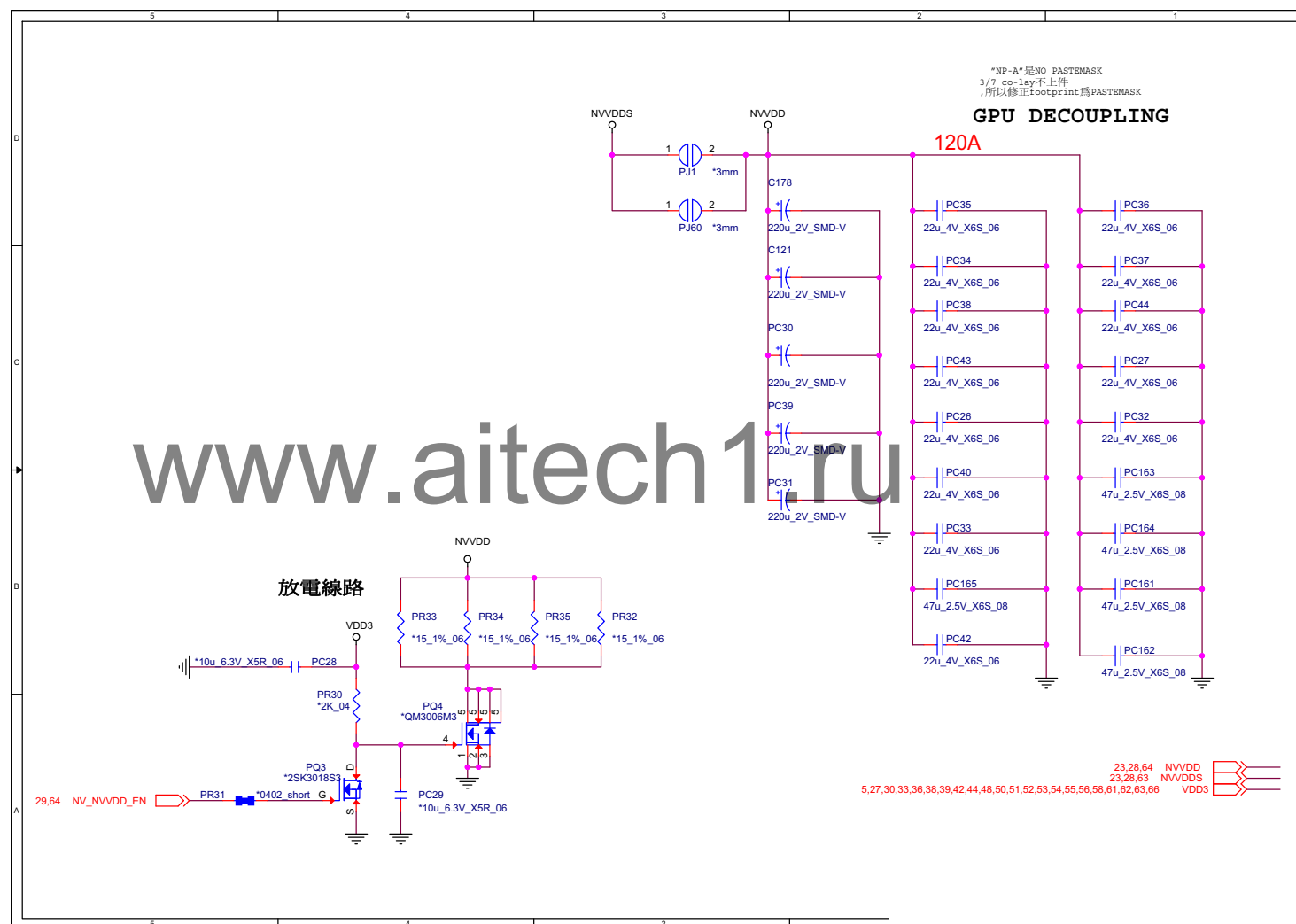
## NVVDDS

Sheet 63 of 74  
NVVDDS

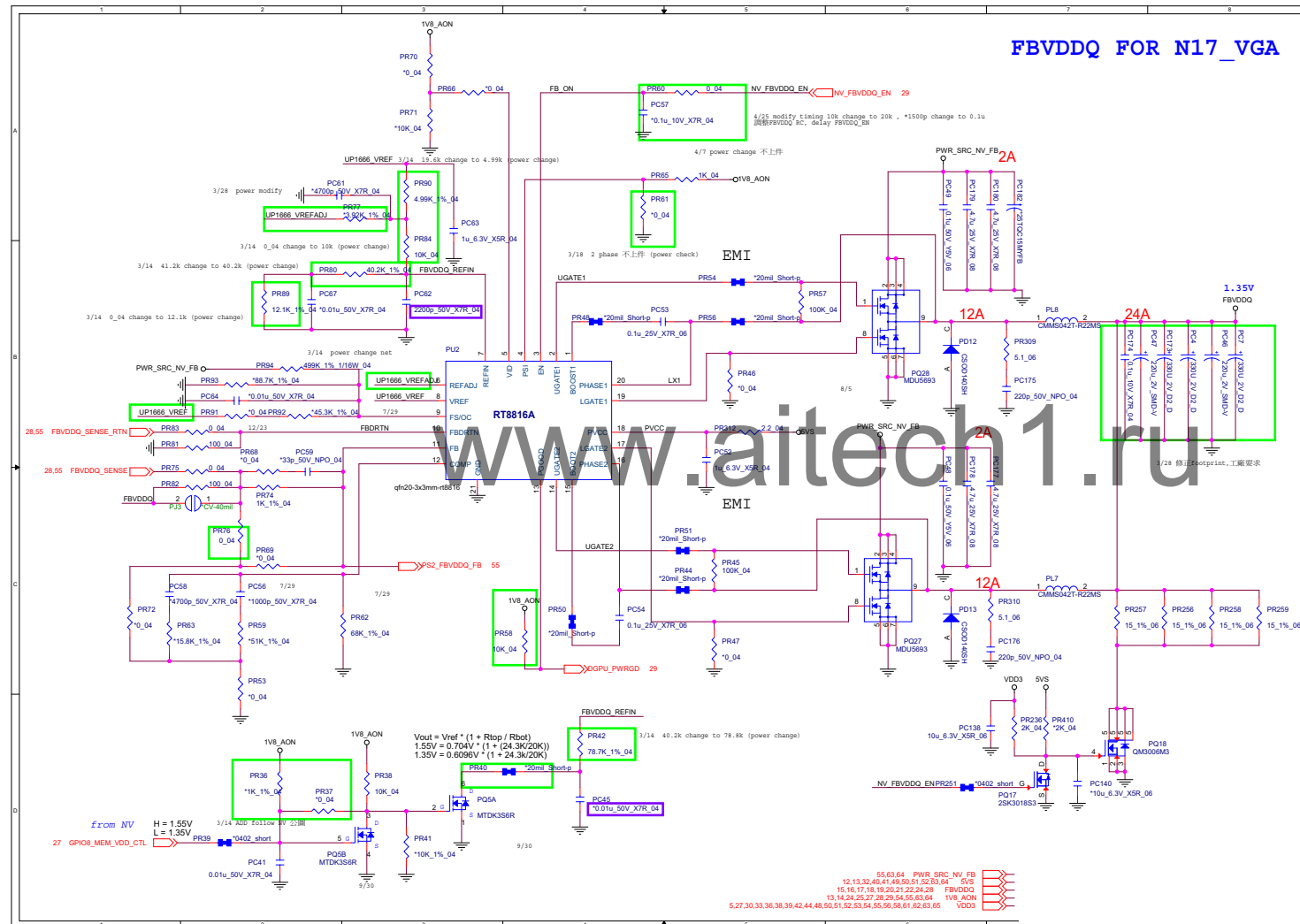
## NVVDD 1

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NVVDD 1

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NVVDD 2

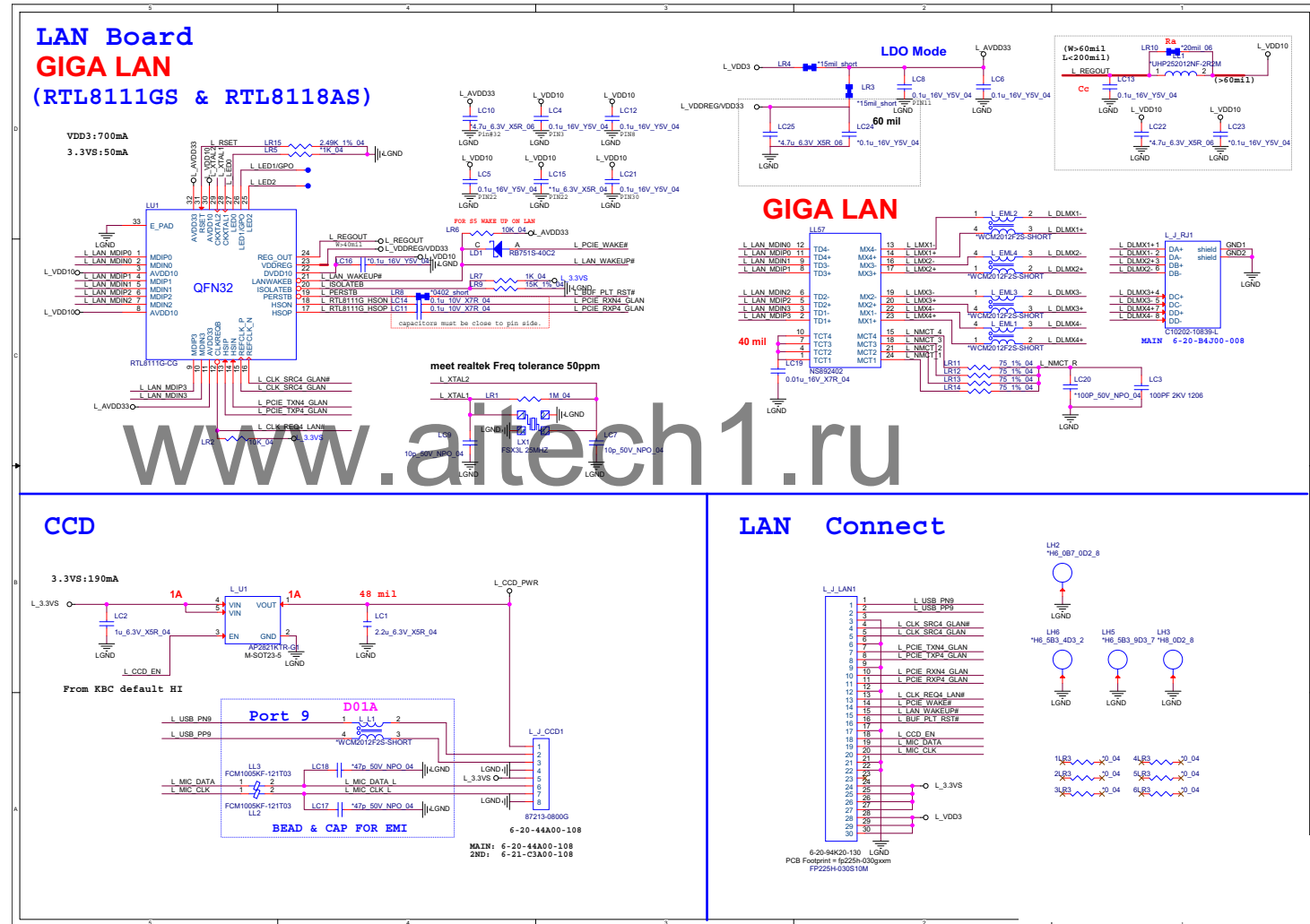


## FBVDDQ B - 67

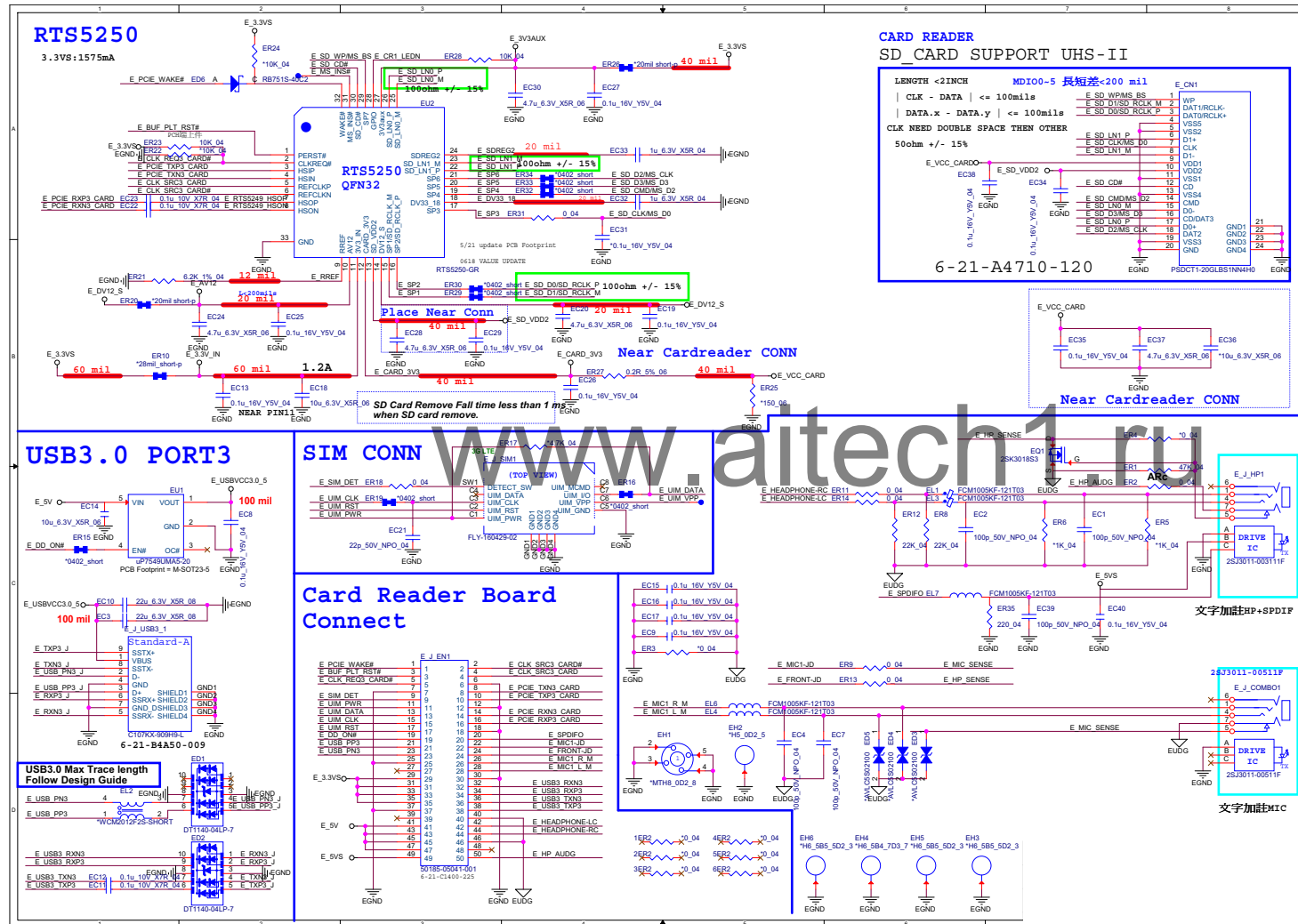


# LAN Board

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LAN Board

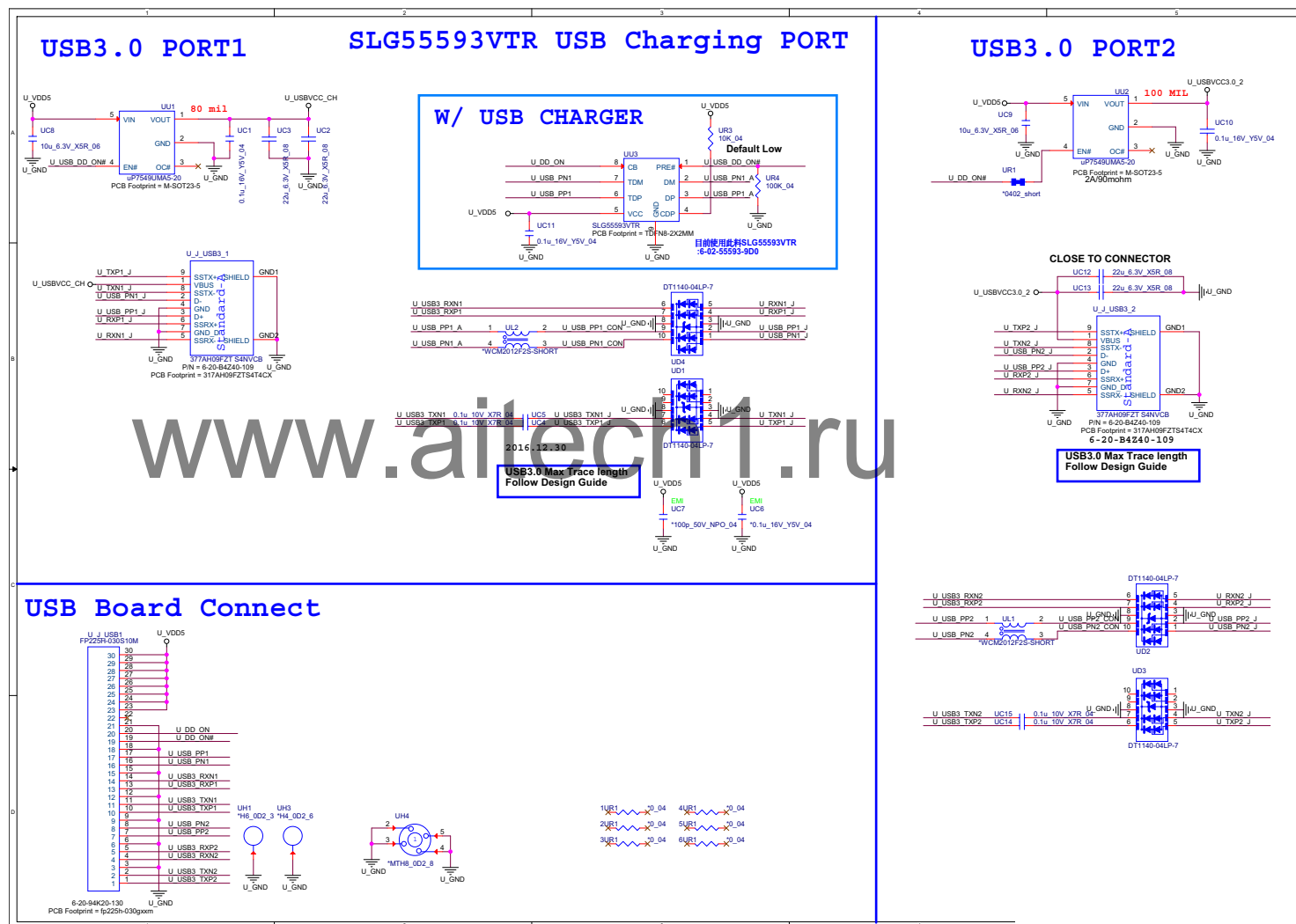


**Reader Board B - 69**

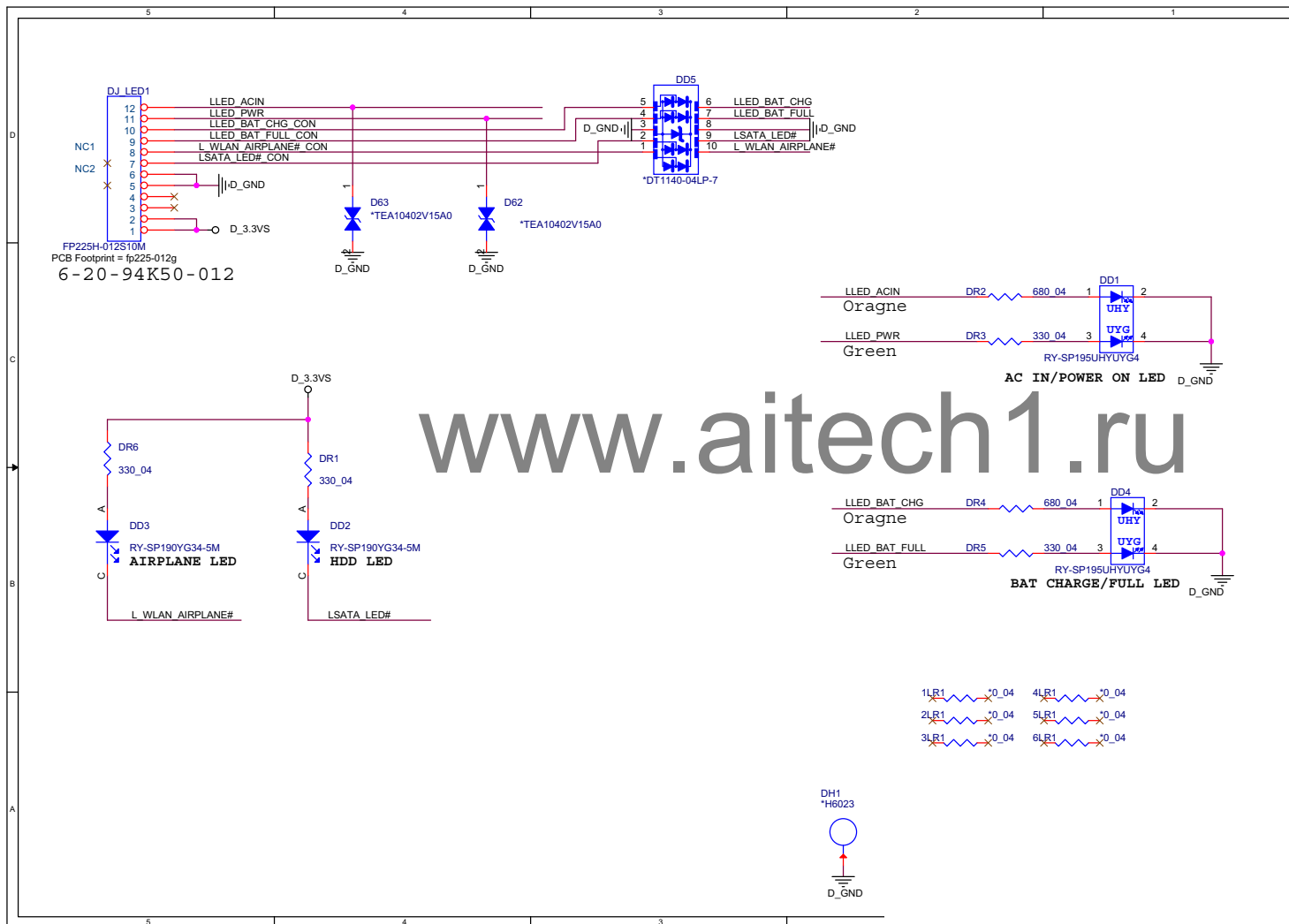


## USB Board

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**USB Board**

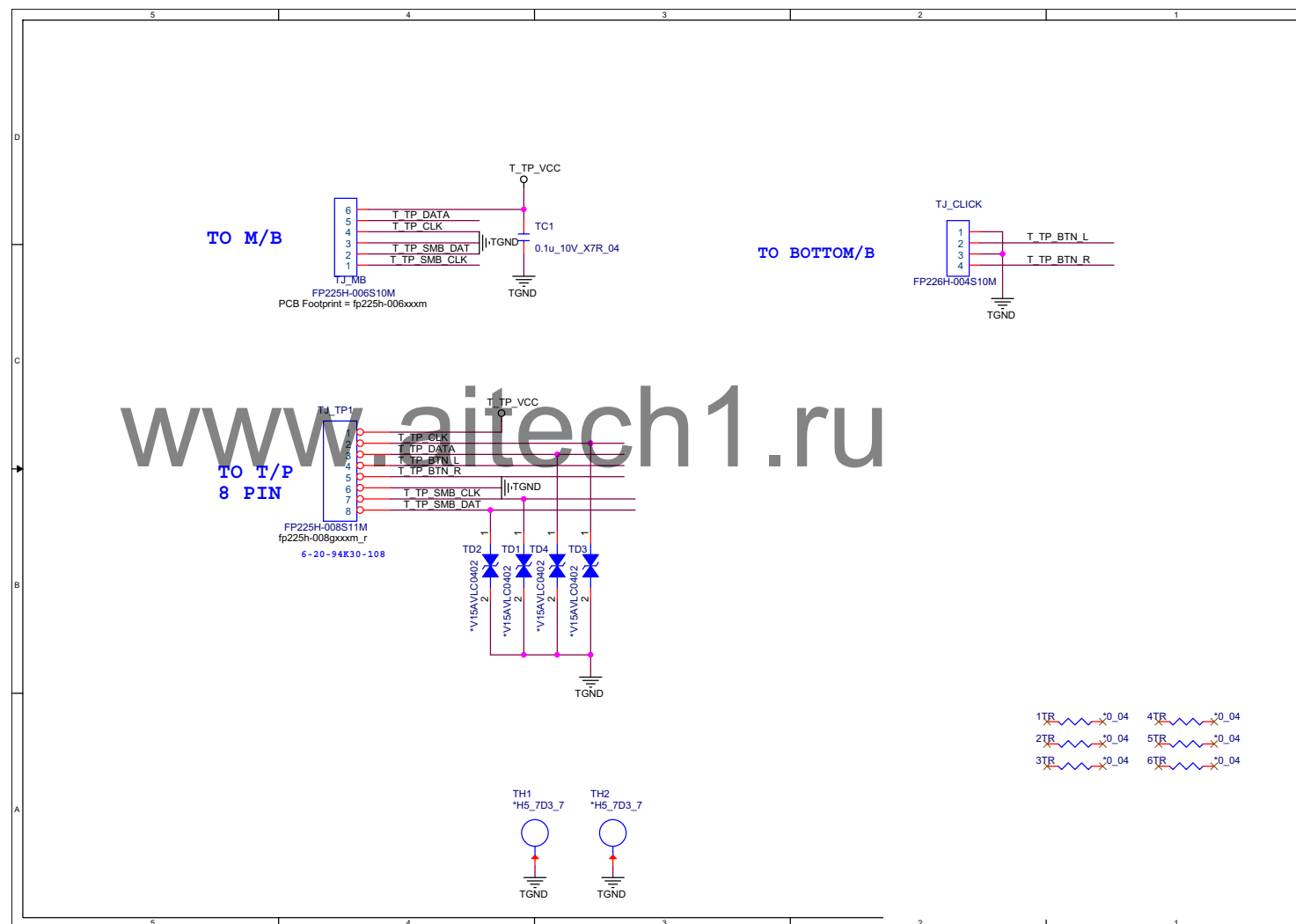


## LED Board

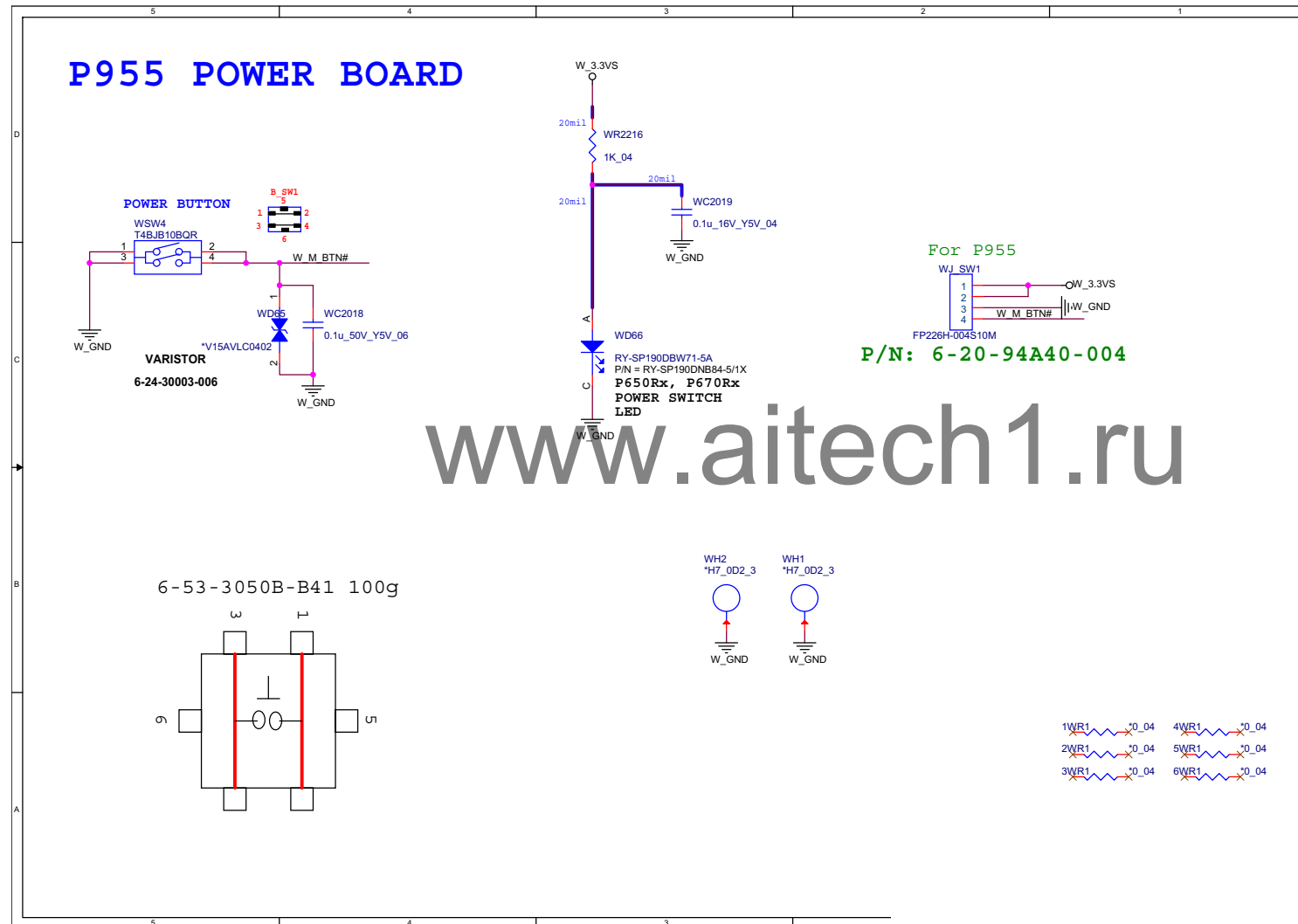


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LED Board

**Sheet 71 of 74**  
**Click Board**



## Power Board

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Power Board

Power Sequence

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Power Sequence



## USB Board B - 75

## B.Schematic Diagrams



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